Rockchip RK1808 Datasheet

Revision 1.0
Sep. 2018

Revision History

Date	Revision	Description
2018-9-13	1.0	Initial released

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Chapter 1 Introduction

1.1 Overview

RK1808 is a high-performance, low power processor for neural network inference. Especially, it is one of current leading solution for mobile device by providing complementary neural network hardware accelerator.
Equipped with one powerful neural network process unit(NPU), it makes RK1808 easy programming and compatible with almost all common development platform like caffe, tensor flow, and so on.
It also integrates a power-efficiency dual-core Cortex-A35 for software flexibility and compatibility.
Many embedded powerful hardware engines are provided to optimize performance for high-end application. RK1808 supports almost full-format H.264 decoder by 1080p@60fps, also support H.264 encoder by 1080p@30fps, high-quality JPEG encoder/decoder.
RK1808 has abundant connectivity interface, like: PCIe 2.1 x2, USB3.0, USB2.0, 1000M Ethernet interface,. etc.
RK1808 has high-performance external memory interface (DDR3/DDR3L/LPDDR2/LPDDR3) capable of sustaining demanding memory bandwidths.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 Microprocessor

- Dual-core ARM Cortex-A35 CPU
- Full implementation of the ARM architecture v8-A instruction set
- ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Include VFP v4 hardware to support single and double-precision operations
- 128KB unified system L2 cache
- Integrated 32KB L1 instruction cache, 32KB L1 data cache with 4-way set associative
- TrustZone technology supported
- One isolated voltage domain to support DVFS
- Separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenario
  - PD_CPU0: 1st Cortex-A35 + Neon + FPU + L1 I/D Cache
  - PD_CPU1: 2nd Cortex-A35 + Neon + FPU + L1 I/D Cache
- One isolated voltage domain to support DVFS

1.2.2 Neural Process Unit

- Support 1920 Int8 MAC operations per cycle
- Support 64 FP16 MAC operations per cycle
- Support 192 Int16 MAC operations per cycle
- 512KB internal buffer
- One isolated voltage domain to support DVFS

1.2.3 Memory Organization

- Internal on-chip memory
  - BootRom
  - SYSTEM_SRAM in the voltage domain of VD_LOGIC
  - PMU_SRAM in the voltage domain of VD_PMU for low power application

- External off-chip memory interface
  - DDR3/DDR3L/LPDDR2/LPDDR3①

- Serial NAND/NOR FLASH
- eMMC
- SD Card

1.2.4 On Chip Memory

- Internal BootRom
  - Used for storing boot code and support system boot from the following interface:
    - SFC interface
    - eMMC interface
    - SDMMC interface
    - SPI2APB interface(SPI2APB also refer as SPI0)
    - USB OTG interface

- SYSTEM_SRAM
  - Size: 2MB

- PMU_SRAM
  - Size: 8KB

1.2.5 External Memory or Storage device

- Dynamic Memory Interface (DDR3/DDR3L/LPDDR2/LPDDR3)
  - Compatible with JEDEC standards
  - Compatible with DDR3-1600/DDR3L-1600/ LPDDR2-1066 /LPDDR3-1600
  - Support 32-bit data width, 2 ranks (chip selects), max 2GB addressing space per rank, total addressing space is 2GB(max)
  - Low power modes, such as power-down and self-refresh for SDRAM

- eMMC interface
  - Compatible with eMMC specification 4.41, 4.51
  - Compatible with standard iNAND interface
  - Support data bus width: 1-bit, 4-bit or 8-bit
  - Support up to 150MB/s data transfer rates

- SD/MMC interface
  - Compatible with SD3.0, MMC ver4.51
  - Data bus width is 4bits

- Serial FLASH interface
  - Support transfer data from/to serial FLASH device
  - Support x1,x2,x4 data bits mode
  - Support 1 chip select

1.2.6 System Component

- CRU (clock & reset unit)
  - One oscillator with 24MHz clock input
  - Provide clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component

- PMU(Power Management Unit)
  - Manage on operating on 4 separate voltage domains for the digital logic circuit: VD_CORE/VD_LOGIC/VD_NPU/VD_PMU
  - Provide powering up/down function for 7 power domains, which are included in the 4 voltage domains independently, to save power.

- Timer
  - Support 6 64bits timers with interrupt-based operation for non-secure application

- Support 2 64bits timers with interrupt-based operation for secure application
- Support two operation modes: free-running and user-defined count
- Support timer work state checkable

- PWM
  - Support 11 on-chip PWMs(PWM0~PWM3,PWM5~PWM11) with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode
  - Optimized for IR receiving application for PWM3, PWM7 and PWM11

- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period
  - One Watchdog for non-secure application
  - One Watchdog for secure application

- Interrupt Controller
  - ARM GIC-500 architecture
  - Support 256 SPI interrupt sources input from different components
  - Support 16 software-triggered interrupts
  - Two interrupt outputs (nFIQ and nIRQ) separately for each Cortex-A35, both are low-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - One embedded DMA controller for system
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable
  - DMAC features:
    - Support 8 channels
    - 31 hardware request from peripherals
    - 2 interrupt output
    - Dual APB slave interface for register configuration, designated as secure and non-secure
    - Support TrustZone technology and programmable secure state for each DMA channel

- Trusted Execution Environment system
  - Support TrustZone technology for the following components

- Cortex-A35, support secure and non-secure mode, switch by software
- System general DMAC, support dedicated channels work only in secure mode
- Secure eFUSE, only can be accessed by Cortex-A35 in secure mode
- SYSTEM_SRAM, part of space is addressed only in secure mode, specific size is software-programmable
- Firewall is embedded to manage other master/slave module

- Cipher engine
  - Support SHA-1, SHA-256/224, SHA-512/384, MD5 with hardware padding
  - Support Link List Item (LLI) DMA transfer
  - Support SHA-1, SHA-256/224,MD5 with hardware padding
  - Support HMAC of SHA-1, SHA-256, MD5 with hardware padding
  - Support AES-128 encrypt & decrypt cipher
  - Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS mode
  - Support up to 4096 bits PKA mathematical operations for RSA/ECC
  - Support up to 8-channels configuration
  - Support Up to 256 bits TRNG output
- Support data scrambling for DDR3/DDR3L/LPDDR3/LPDDR2
- Support secure debug

1.2.7 Video CODEC

- Video Decoder
  - H.264/AVC Base/Main/High@level4.2; up to 1080p@60fps

- Video Encoder
  - Support H.264 video encoder at BP/MP/HP@level4.2
  - 1920p@30FPS
  - 1x1080p@30fps or 2x720p@30fps encoding

1.2.8 JPEG CODEC

- JPEG decoder
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Support JPEG ROI (region of image) decode
- JPEG encodeer
  - Baseline (DCT sequential)

1.2.9 Graphic Engine

- 2D Graphics Engine:
  - Data format
    - Support input of ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422
    - Support input of YUV422SP10bit/YUV420SP10bit(YUV-8bits out)
    - Support output of ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422
    - Pixel Format conversion, BT.601/BT.709
    - Dither operation
    - Max resolution: 8192x8192 source, 4096x4096 destination
  - Scaling
    - Down-scaling: Average filter
    - Up-scaling: Bi-cubic filter(source>2048 would use Bi-linear)
    - Arbitrary non-integer scaling ratio，from 1/8 to 8
  - Rotation
    - 0, 90, 180, 270 degree rotation
    - x-mirror, y-mirror& rotation operation
  - BitBLT
    - Block transfer
    - Color palette/Color fill, support with alpha
    - Transparency mode (color keying/stencil test, specified value/value range)
    - Two source BitBLT:
    - A+B=B only BitBLT, A support rotate&scale when B fixed

- A+B=C second source (B) has same attribute with (C) plus rotation function
- Alpha Blending
  - New comprehensive per-pixel alpha(color/alpha channel separately)
  - Fading
  - SRC1(R2Y)&&SRC0(YUV)—alpha->DST(YUV)

1.2.10 Video input interface

- Interface and video input processor
  - Support up to 16bit DPI interface (digital parallel input)
  - Support up MIPI CSI RX interface
  - Support CIF block(Camera Interface)
  - Support ISP block(Image Signal Processor)
  - Support DPI interface to CIF block
  - Support DPI interface to ISP block
  - Support MIPI CSI RX interface to ISP block
  - Support the following two mode simultaneously
    - DPI interface with VIP
    - MIPI CSI RX interface with ISP

- DPI Interface
  - Support 8bit/10bit/12bit/16bit input
  - Support up to 150MHz input data

- MIPI CSI RX Interface
  - Compatible with the MIPI Alliance Interface specification v1.0
  - Up to 4 data lane, 2.0Gbps maximum data rate per lane
  - Support MIPI-HS, MIPI-LP mode

- CIF
  - Support BT601 YCbCr 422 8bit input
  - Support BT656 YCbCr 422 8bit input
  - Support UYVY/VYUY/YUYV/YVYU configurable
  - Support RAW 8/10/12 bit input
  - Support JPEG input
  - Support BT1120 16bit,single/dual-edge sampling
  - Support receiving CSI2 protocol data(up to four IDs)
  - Support receiving DSI protocol data(Video mode/Command mode)
  - Support window cropping
  - Support virtual stride when write to DDR
  - Support different stored address for Y and UV
  - Support 422/420 output
  - Support the polarity of pixel_clk、hsync、vsync configurable

- ISP
  - Generic Sensor Interface with programmable polarity for synchronization signals
  - ITU-R BT 601/656 compliant video interface supporting YCbCr or RGB Bayer data
  - 12 bit camera interface
  - 12 bit resolution per color component internally
  - YCbCr 4:2:2 processing
  - FLASH light control
  - Mechanical shutter support
  - Windowing and frame synchronization
  - Macro block line, frame end, capture error, data loss interrupts and sync. (h_start, v_start) interrupts
  - Luminance/chrominance and chrominance blue/red swapping for YUV input signals
  - Continuous resize support
  - Semi planar storage format

- Color processing (contrast, saturation, brightness, hue, offset, range)
- Power management by software controlled clock disabling of currently not needed sub-modules
- Four channel Lens shade correction(Vignetting)
- Auto focus measurement
- White balancing and black level measurement
- Auto exposure support by brightness measurement i5x5 sub windows
- Defect pixel cluster correction unit (DPCC) supports othe fly
- De-noising pre filter (DPF)
- Enhanced color interpolation (RGB Bayer demosaicing)
- Chromatic aberration correction
- Combined edge sensitive Sharpening / Blurring filter (Noise filter)
- Color correction matrix (cross talk matrix)
- Flexible Histogram calculation
- Digital image effects (Emboss, Sketch, Sepia, B/W (Grayscale), Color Selection, Negative image, sharpening)
- Solarize effect through gamma correction
- Maximum input resolution of 1920x1080 pixels
- Main scaler with pixel-accurate up- and down-scaling to any resolutiobetwee1920x1080 and 32x16 pixel in processing mode
- Self scaler with pixel-accurate up- and down-scaling to any resolutiobetwee1920x1080 and 32x16 pixel in processing mode
- Support of semi-planar NV21 color storage format
- Support of image cropping
- Support Y12BIT and UV 8BIT path output after GAMMAOUT module
- Support RGB output after GAMMAOUT module
- Support hurry for latency FIFO
- Support 128bit AXI and MMU interface

1.2.11 Display interface

- Parallel output interface
  - Up to 720p@60fps display output
  - Maximum with 18bit output data
  - Compatible with RGB and MCU mode

- MIPI DSI interface
  - Compatible with MIPI Alliance Interface specification v1.0
  - Support 4 data lane, 2.0Gbps maximum data rate per lane
  - Up to 1080p@60fps display output

1.2.12 Video Output Processor LITE(VOP_LITE)

- Display interface
  - Parallel output Interface:18-bit(RGB666), 16-bit(RGB565)
  - MIPI DSI interface
  - MCU interface
  - Max output resolution
    - 1920x1080 for MIPI
    - 1280x800 for RGB
- Display process
  - Background layer
    - programmable 24-bit color
  - Win1 layer
    - RGB888, ARGB888, RGB565
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
- Others

- Support dither down allegro RGB888to666 RGB888to565 &
- Support dither down frc (configurable) RGB888to666
- Blank and black display
- Standby mode
- Support DMA stop mode

1.2.13 Video Output Processor RAW(VOP_RAW)

- Display interface
  - Parallel RGB Interface
  - Parallel PDAF Interface
  - Max output resolution:5k(16M cam)
  - Support max timing 8k
- Layer process
  - Background layer
    - Programmable 10bit raw
  - Win layer
    - Support data format : RAW8/RAW10/RAW16
    - Support virtual display
    - Master address 64bit aligned
- Others
  - Support ping-pong mode
  - PDAF support Hblank/Vblank/interleave mode

1.2.14 Audio Interface

- I2S0 with 8 channel
  - Up to 8 channels TX and 8 channels RX path
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
  - Support configured as I2S mode or PCM mode

- I2S1 with 2 channel
  - Up to 2 channels for TX and 2 channels RX path
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
  - Support configured as I2S mode or PCM mode

- PDM
  - Up to 8 channels
  - Audio resolution from 16bits to 24bits
  - Sample rate up to 192KHz
  - Support PDM master receive mode

- TDM
  - supports up to 8 channels for TX and 8 channels RX path
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)

- Voice Activity Detection(VAD)

- Support read voice data from I2S/PDM
- Support voice amplitude detection
- Support Multi-Mic array data storing
- Support a level combined interrupt

1.2.15 Connectivity

- SDIO interface
  - Compatible with SDIO3.0 protocol
  - 4bits data bus widths

- GMAC 10/100/1000M ethernet controller
  - Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces
  - Supports 10/100-Mbps data transfer rates with the RMII interfaces
  - There are 2 controllers, one is connected to internal FE PHY, the other is for external PHY device
  - Supports both full-duplex and half-duplex operation
    - Supports CSMA/CD Protocol for half-duplex operation
    - Supports packet bursting and frame extension in 1000 Mbps half-duplex operation
    - Supports IEEE 802.3x flow control for full-duplex operation
    - Optional forwarding of received pause control frames to the user application in full-duplex operation
    - Back-pressure support for half-duplex operation
    - Automatic transmission of zero-quanta pause frame on de-assertion of flow control input in full-duplex operation
  - Preamble and start-of-frame data (SFD) insertion in Transmit, and deletion in Receive paths
  - Automatic CRC and pad generation controllable on a per-frame basis
  - Options for Automatic Pad/CRC Stripping on receive frames
  - Programmable Inter-Frame-Gap (40-96 bit times in steps of 8)
  - Supports a variety of flexible address filtering modes
  - Separate 32-bit status returned for transmission and reception packets
  - Supports IEEE 802.1Q VLAN tag detection for reception frames
  - Support detection of LAN wake-up frames and AMD Magic Packet frames
  - Support checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame
  - Support checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagram
  - Comprehensive status reporting for normal operation and transfers with errors
  - Automatic generation of PAUSE frame control or backpressure signal to the GMAC core based on Receive FIFO-fill (threshold configurable) level
  - Handles automatic retransmission of Collision frames for transmission
  - Discards frames on late collision, excessive collisions, excessive deferral and under-run conditions

- USB 2.0 Host
  - Compatible with USB 2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Support Open Host Controller Interface Specification (OHCI), Revision 1.0a

- USB OTG3.0
  - Compatible Specification
    - Universal Serial Bus 3.0 Specification, Revision 1.0
    - Universal Serial Bus Specification, Revision 2.0
    - Extensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
  - Support Control/Bulk (including stream)/Interrupt/Isochronous Transfer

- Simultaneous IN and OUT transfer for USB3.0, up to 8Gbps bandwidth
- Descriptor Caching and Data Pre-fetching

- PCIe interface②
  - Compatible with PCI Express Base Specification Revision 2.1
  - Dual operation mode: Root Complex(RC)and End Point(EP)
  - Maximum link width is 2, single bi-directional Link interface
  - Maximum Payload Size of 128 bytes
  - Maximum 32 Non-Posted outstanding transactions
  - Support 2.5Gbbps and 5.0 Gbps serial data transmission rate per lane per direction

- SPI interface
  - Support 2 SPI Controllers(SPI1/SPI2), one support one chip-select output and the other support two chip-select output
  - Support serial-master and serial-slave mode, software-configurable

- SPI2APB interface(SPI0)
  - Support slave mode SPI protocol
  - Support serial-slave mode only
  - Embedded a APB master interface

- I2C interface
  - Support 6 I2C interfaces(I2C0-I2C5)
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100k bits/s in the Standard-mode, up to 400k bits/s in the Fast-mode or up to 1m bits/s in Fast-mode Plus.

- UART interface
  - Support 8 UART interfaces(UART0-UART7)
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode for UART0/UART1/UART3/UART4/UART5

1.2.16 Others

- Multiple group of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction(a weak pull-up and a weak pull-down)
  - Support configurable drive strength

- Temperature sensor(TSADC)
  - -40~125℃ temperature range and 5℃ temperature resolution

- Successive approximation ADC (SARADC)
  - 10-bit resolution
  - Up to 1MS/s sampling rate
  - 4 single-ended input channels

- eFUSE
  - Support 2K bit Size, 1K bit for secure application, the other for non-secure
  - Support Program/Read/Idle mode

- Package type
  - FCCSP 420-pin(body: 14mm x 14mm; ball size: 0.3mm)

Notes:

① : DDR3/DDR3L/LPDDR2/LPDDR3 are not used simultaneously

② : PCIe/USB3 are not used simultaneously

1.3 Block Diagram

The following diagram shows the basic block diagram.

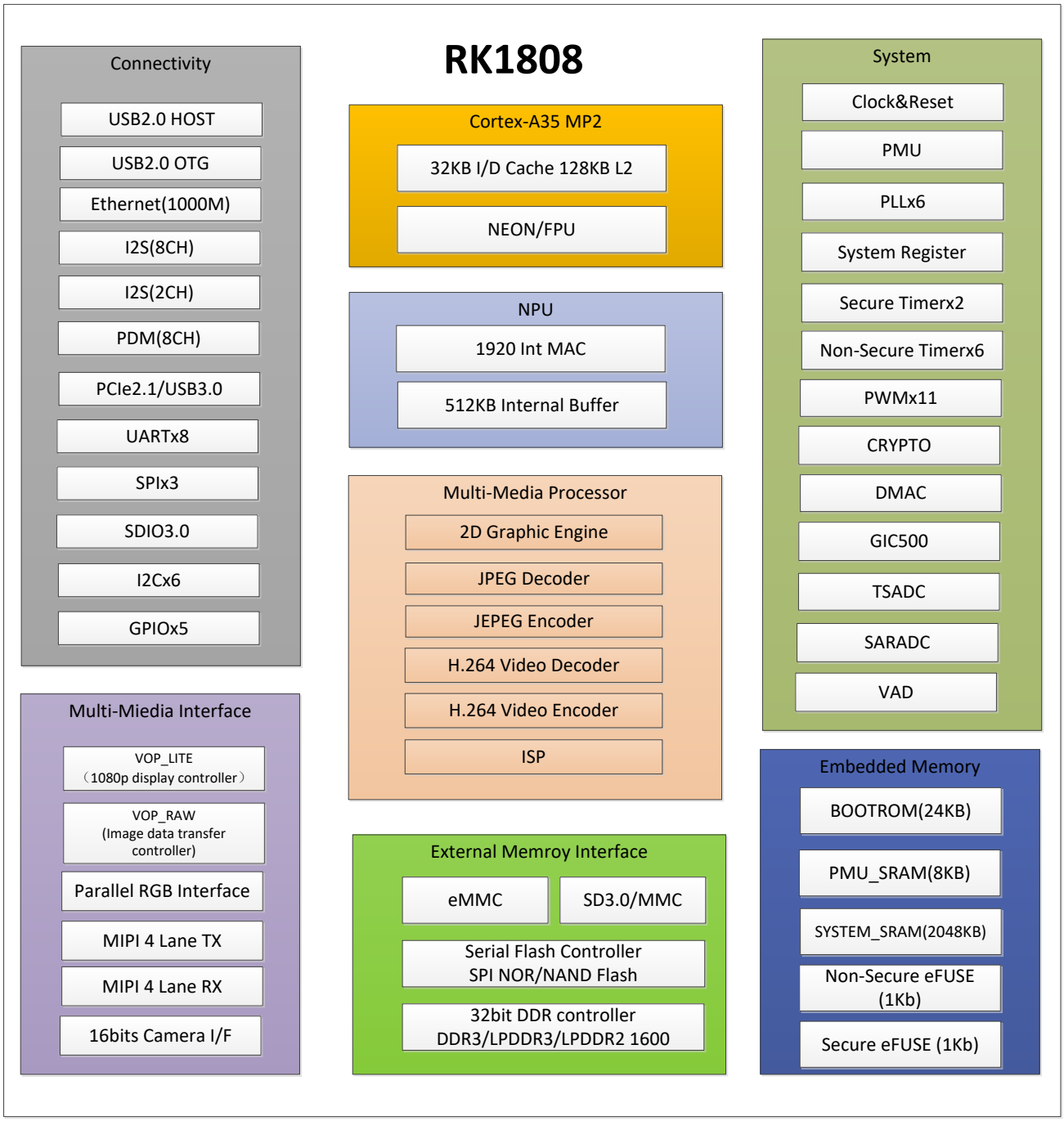

Fig.1-1 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK1808	RoHS	FCCSP420LD	1190	Dual core application processor

2.2 Top Marking

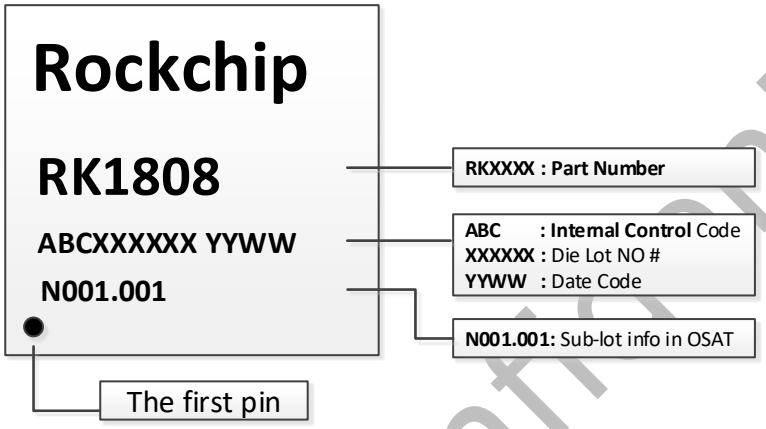

Fig.2-1 Package definition

2.3 FCCSP 420L Dimension

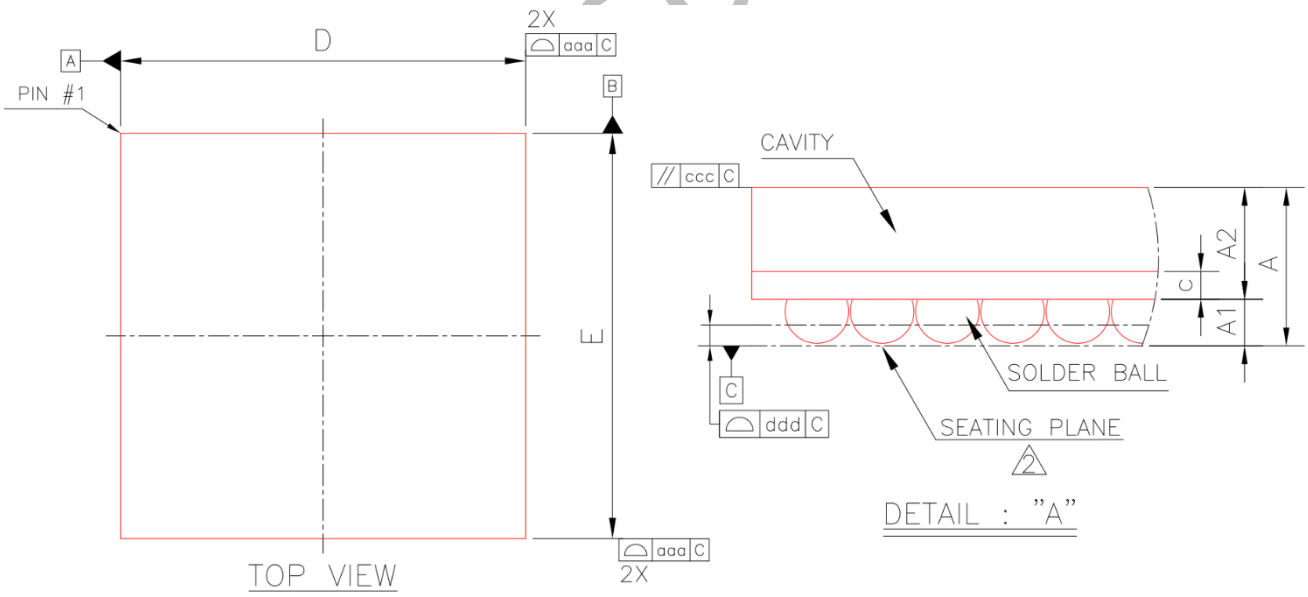

Fig.2-2 Package Top And Side View

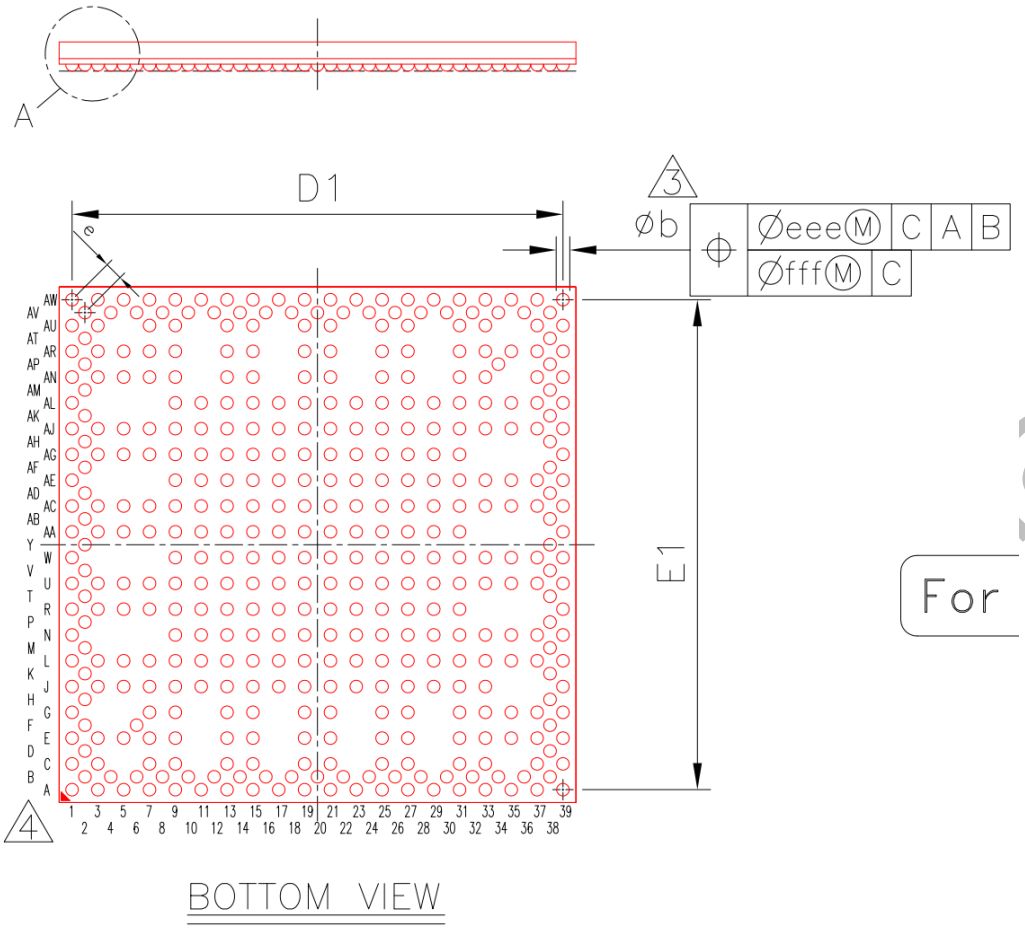

Fig.2-3 Package bottom view

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.735	0.805	0.875	0.029	0.032	0.034
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.545	0.595	0.645	0.021	0.023	0.025
c	0.125	0.145	0.165	0.005	0.006	0.006
D	13.900	14.000	14.100	0.547	0.551	0.555
E	13.900	14.000	14.100	0.547	0.551	0.555
D1	---	13.300	---	---	0.524	---
E1	---	13.300	---	---	0.524	---
e	---	0.495	---	---	0.019	---
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.150			0.006		
ccc	0.200			0.008		
ddd	0.100			0.004		
eee	0.150			0.006		
fff	0.050			0.002		
MD/ME	39 / 39					

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .
5. SPECIAL CHARACTERISTICS C CLASS: ccc, ddd
6. REFERANCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5
7. BALL PLACEMENT USE 0.30 mm SOLDER BALL. BGA PAD SOLDER MASK OPENING = 0.275 mm.

Fig.2-4 Package dimension

2.4 Ball Map

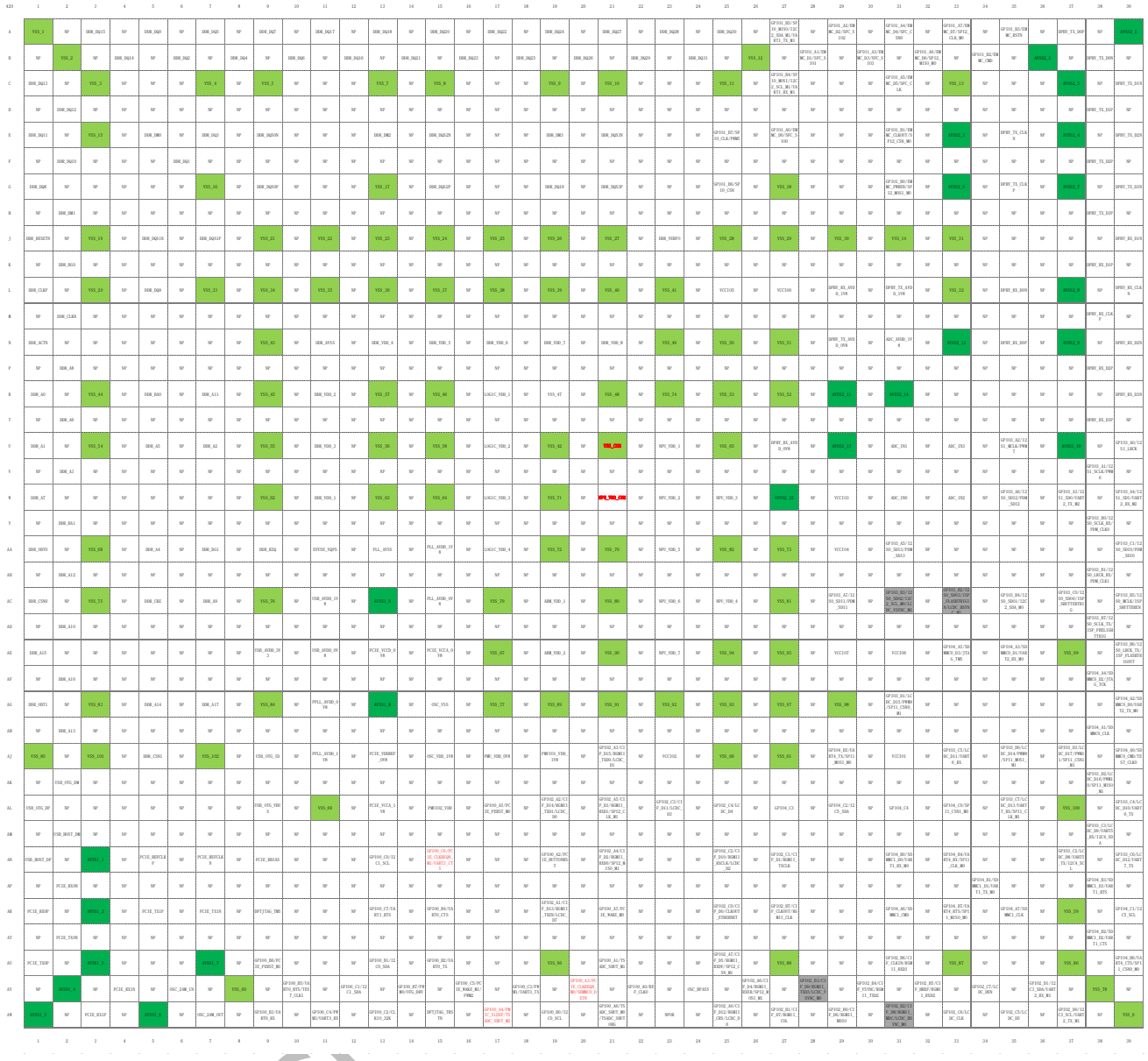

Fig.2-5 Ball Map

2.5 Pin Number List

Table 2-1 Pin Number Order Information

Pin name	Pin#	Pin name	Pin#
VSS_1	A1	PCIE_RX1P	AW3
DDR_DQ15	A3	AVSS1_6	AW5
DDR_DQ0	A5	OSC_24M_OUT	AW7
DDR_DQ5	A7	GPIO0_B3/UART0_RX	AW9
DDR_DQ7	A9	GPIO0_C4/PWM3/UART3_RX	AW11
DDR_DQ17	A11	GPIO0_C2/CLKIO_32K	AW13
DDR_DQ18	A13	DFTJTAG_TRSTN	AW15
DDR_DQ20	A15	GPIO0_A4/PMIC_SLEEP/TSADC_SHUT_M2	AW17
DDR_DQ22	A17	GPIO0_B0/I2C0_SCL	AW19
DDR_DQ24	A19	GPIO0_A6/TSADC_SHUT_M0/TSADC_SHUTORG	AW21
DDR_DQ27	A21	NPOR	AW23
DDR_DQ28	A23	GPIO2_A0/CIF_D12/RGMII_CRS/LCDC_D6	AW25
DDR_DQ30	A25	GPIO2_B1/CIF_D7/RGMII_COL	AW27
GPIO1_B5/SPI0_MISO/I2C2_SDA_M1/UART1_TX_M1	A27	GPIO2_B0/CIF_D6/RGMII_MDIO	AW29
GPIO1_A2/EMMC_D2/SFC_SIO2	A29	GPIO2_B2/CIF_D8/RGMII_MDC/LCDC_HSYNC_M0	AW31
GPIO1_A4/EMMC_D4/SFC_CSN0	A31	GPIO2_C6/LCDC_CLK	AW33
GPIO1_A7/EMMC_D7/SPI2_CLK_M0	A33	GPIO2_C5/LCDC_D5	AW35
GPIO1_B3/EMMC_RSTN	A35	GPIO2_D0/I2C3_SCL/UART2_TX_M1	AW37
DPHY_TX_D0P	A37	VSS_6	AW39
AVSS2_1	A39	VSS_2	B2
DDR_ODT0	AA1	DDR_DQ14	B4
VSS_68	AA3	DDR_DQ2	B6
DDR_A4	AA5	DDR_DQ4	B8
DDR_BG1	AA7	DDR_DQ6	B10
DDR_RZQ	AA9	DDR_DQ16	B12
EFUSE_VQPS	AA11	DDR_DQ21	B14
PLL_AVSS	AA13	DDR_DQ23	B16
PLL_AVDD_1V8	AA15	DDR_DQ25	B18
LOGIC_VDD_4	AA17	DDR_DQ26	B20
VSS_72	AA19	DDR_DQ29	B22
VSS_70	AA21	DDR_DQ31	B24
NPU_VDD_5	AA23	VSS_12	B26
VSS_82	AA25	GPIO1_A1/EMMC_D1/SFC_SIO1	B28
VSS_73	AA27	GPIO1_A3/EMMC_D3/SFC_SIO3	B30
VCCIO4	AA29	GPIO1_A6/EMMC_D6/SPI2_MISO_M0	B32
GPIO3_A5/I2S0_SDI3/PDM_SDI3	AA31	GPIO1_B2/EMMC_CMD	B34
GPIO3_C1/I2S0_SDI0/PDM_SDI0	AA39	AVSS2_2	B36
DDR_A12	AB2	DPHY_TX_D0N	B38
GPIO3_B1/I2S0_LRCK_RX/PDM_CLK1	AB38	DDR_DQ13	C1
DDR_CSN0	AC1	VSS_3	C3
VSS_75	AC3	VSS_4	C7
DDR_CKE	AC5	VSS_5	C9

Pin name	Pin#	Pin name	Pin#
DDR_A9	AC7	VSS_7	C13
VSS_76	AC9	VSS_8	C15
USB_AVDD_1V8	AC11	VSS_9	C19
AVSS1_9	AC13	VSS_10	C21
PLL_AVDD_0V8	AC15	VSS_11	C25
VSS_79	AC17	GPIO1_B4/SPI0_MOSI/I2C2_SCL_M1/UART1_RX_M1	C27
ARM_VDD_1	AC19	GPIO1_A5/EMMC_D5/SFC_CLK	C31
VSS_80	AC21	VSS_13	C33
NPU_VDD_6	AC23	AVSS2_5	C37
NPU_VDD_4	AC25	DPHY_TX_D1N	C39
VSS_81	AC27	DDR_DQ12	D2
GPIO3_A7/I2S0_SDI1/PDM_SDI1	AC29	DPHY_TX_D1P	D38
GPIO3_B3/I2S0_SDO2/I2C2_SCL_M0/LCDC_VSYNC_M1	AC31	DDR_DQ11	E1
GPIO3_B2/I2S0_SDO3/ISP_FLASHTRIGIN/LCDC_HSYNC_M1	AC33	VSS_15	E3
GPIO3_B4/I2S0_SDO1/I2C2_SDA_M0	AC35	DDR_DM0	E5
GPIO3_C0/I2S0_SDO0/ISP_SHUTTERTRIG	AC37	DDR_DQ3	E7
GPIO3_B5/I2S0_MCLK/ISP_SHUTTEREN	AC39	DDR_DQS0N	E9
DDR_A10	AD2	DDR_DM2	E13
GPIO3_B7/I2S0_SCLK_TX/ISP_PRELIGHTTRIG	AD38	DDR_DQS2N	E15
DDR_A15	AE1	DDR_DM3	E19
USB_AVDD_3V3	AE9	DDR_DQS3N	E21
USB_AVDD_0V8	AE11	GPIO1_B7/SPI0_CLK/PWM5	E25
PCIE_VCCD_0V8	AE13	GPIO1_A0/EMMC_D0/SFC_SIO0	E27
PCIE_VCCA_0V8	AE15	GPIO1_B1/EMMC_CLKOUT/SPI2_CSN_M0	E31
VSS_67	AE17	AVSS2_3	E33
ARM_VDD_2	AE19	DPHY_TX_CLKN	E35
VSS_90	AE21	AVSS2_4	E37
NPU_VDD_7	AE23	DPHY_TX_D2N	E39
VSS_94	AE25	DDR_DQ10	F2
VSS_95	AE27	DDR_DQ1	F6
VCCIO7	AE29	DPHY_TX_D2P	F38
VCCIO6	AE31	DDR_DQ8	G1
GPIO4_A5/SDMMC0_D3/JTAG_TMS	AE33	VSS_16	G7
GPIO4_A3/SDMMC0_D1/UART2_RX_M0	AE35	DDR_DQS0P	G9
VSS_99	AE37	VSS_17	G13
GPIO3_B6/I2S0_LRCK_TX/ISP_FLASHTRIGOUT	AE39	DDR_DQS2P	G15
DDR_A16	AF2	DDR_DQ19	G19
GPIO4_A4/SDMMC0_D2/JTAG_TCK	AF38	DDR_DQS3P	G21
DDR_ODT1	AG1	GPIO1_B6/SPI0_CSN	G25
VSS_83	AG3	VSS_18	G27
DDR_A14	AG5	GPIO1_B0/EMMC_PWREN/SPI2_MOSI_M0	G31
DDR_A17	AG7	AVSS2_6	G33
VSS_84	AG9	DPHY_TX_CLKP	G35
PPLL_AVDD_0V8	AG11	AVSS2_7	G37

Pin name	Pin#	Pin name	Pin#
AVSS1_8	AG13	DPHY_TX_D3N	G39
OSC_VSS	AG15	DDR_DM1	H2
VSS_77	AG17	DPHY_TX_D3P	H38
VSS_89	AG19	DDR_RESETN	J1
VSS_91	AG21	VSS_19	J3
VSS_92	AG23	DDR_DQS1N	J5
VSS_93	AG25	DDR_DQS1P	J7
VSS_97	AG27	VSS_21	J9
VSS_98	AG29	VSS_22	J11
GPIO3_D1/LCDC_D15/PWM9/SPI1_CSN0_M1	AG31	VSS_23	J13
GPIO4_A2/SDMMC0_D0/UART2_TX_M0	AG39	VSS_24	J15
DDR_A13	AH2	VSS_25	J17
GPIO4_A1/SDMMC0_CLK	AH38	VSS_26	J19
VSS_85	AJ1	VSS_27	J21
VSS_101	AJ3	DDR_VERFO	J23
DDR_CSN1	AJ5	VSS_28	J25
VSS_102	AJ7	VSS_29	J27
USB_OTG_ID	AJ9	VSS_30	J29
PPLL_AVDD_1V8	AJ11	VSS_14	J31
PCIE_VDDREF_0V8	AJ13	VSS_31	J33
OSC_VDD_1V8	AJ15	DPHY_RX_D1N	J39
PMU_VDD_0V8	AJ17	DDR_BG0	K2
PMUIO1_VDD_1V8	AJ19	DPHY_RX_D1P	K38
GPIO2_A3/CIF_D15/RGMII_TXD0/LCDC_D1	AJ21	DDR_CLKP	L1
VCCIO2	AJ23	VSS_20	L3
VSS_66	AJ25	DDR_DQ9	L5
VSS_61	AJ27	VSS_33	L7
GPIO4_B5/UART4_TX/SPI1_MOSI_M0	AJ29	VSS_34	L9
VCCIO1	AJ31	VSS_35	L11
GPIO3_C5/LCDC_D11/UART6_RX	AJ33	VSS_36	L13
GPIO3_D0/LCDC_D14/PWM8/SPI1_MOSI_M1	AJ35	VSS_37	L15
GPIO3_D3/LCDC_D17/PWM11/SPI1_CSN1_M1	AJ37	VSS_38	L17
GPIO4_A0/SDMMC0_CMD/TEST_CLK0	AJ39	VSS_39	L19
USB_OTG_DM	AK2	VSS_40	L21
GPIO3_D2/LCDC_D16/PWM10/SPI1_MISO_M1	AK38	VSS_41	L23
USB_OTG_DP	AL1	VCCIO5	L25
USB_OTG_VBUS	AL9	VCCIO0	L27
VSS_69	AL11	DPHY_RX_AVDD_1V8	L29
PCIE_VCCA_1V8	AL13	DPHY_TX_AVDD_1V8	L31
PMUIO2_VDD	AL15	VSS_32	L33
GPIO0_A5/PCIE_PERST_M0	AL17	DPHY_RX_D0N	L35
GPIO2_A2/CIF_D14/RGMII_TXD1/LCDC_D0	AL19	AVSS2_8	L37
GPIO2_A5/CIF_D3/RGMII_RXD1/SPI2_CLK_M1	AL21	DPHY_RX_CLKN	L39
GPIO2_C3/CIF_D11/LCDC_D3	AL23	DDR_CLKN	M2
GPIO2_C4/LCDC_D4	AL25	DPHY_RX_CLKP	M38

Pin name	Pin#	Pin name	Pin#
GPIO4_C3	AL27	DDR_ACTN	N1
GPIO4_C2/I2C5_SDA	AL29	VSS_43	N9
GPIO4_C4	AL31	DDR_AVSS	N11
GPIO4_C0/SPI1_CSN1_M0	AL33	DDR_VDD_4	N13
GPIO3_C7/LCDC_D13/UART7_RX/SPI1_CLK_M1	AL35	DDR_VDD_5	N15
VSS_100	AL37	DDR_VDD_6	N17
GPIO3_C4/LCDC_D10/UART6_TX	AL39	DDR_VDD_7	N19
USB_HOST_DM	AM2	DDR_VDD_8	N21
GPIO3_C3/LCDC_D9/UART5_RX/I2C4_SDA	AM38	VSS_49	N23
USB_HOST_DP	AN1	VSS_50	N25
AVSS1_1	AN3	VSS_51	N27
PCIE_REFCLKP	AN5	DPHY_TX_AVDD_0V8	N29
PCIE_REFCLKN	AN7	ADC_AVDD_1V8	N31
PCIE_RBIAS	AN9	AVSS2_12	N33
GPIO0_C0/I2C1_SCL	AN13	DPHY_RX_D0P	N35
GPIO0_C6/PCIE_CLKREQN_M1/UART3_CTS	AN15	AVSS2_9	N37
GPIO0_A2/PCIE_BUTTONRST	AN19	DPHY_RX_D2N	N39
GPIO2_A4/CIF_D2/RGMII_RXD0/SPI2_MISO_M1	AN21	DDR_A8	P2
GPIO2_C2/CIF_D10/RGMII_RXCLK/LCDC_D2	AN25	DPHY_RX_D2P	P38
GPIO2_C1/CIF_D1/RGMII_TXCLK	AN27	DDR_A0	R1
GPIO4_B0/SDMMC1_D0/UART1_RX_M0	AN31	VSS_44	R3
GPIO4_B4/UART4_RX/SPI1_CLK_M0	AN33	DDR_BA0	R5
GPIO3_C2/LCDC_D8/UART5_TX/I2C4_SCL	AN37	DDR_A11	R7
GPIO3_C6/LCDC_D12/UART7_TX	AN39	VSS_45	R9
PCIE_RX0N	AP2	DDR_VDD_2	R11
GPIO4_B1/SDMMC1_D1/UART1_TX_M0	AP34	VSS_57	R13
GPIO4_B3/SDMMC1_D3/UART1_RTS	AP38	VSS_46	R15
PCIE_RX0P	AR1	LOGIC_VDD_1	R17
AVSS1_2	AR3	VSS_47	R19
PCIE_TX1P	AR5	VSS_48	R21
PCIE_TX1N	AR7	VSS_74	R23
DFTJTAG_TMS	AR9	VSS_53	R25
GPIO0_C7/UART3_RTS	AR13	VSS_52	R27
GPIO0_B4/UART0_CTS	AR15	AVSS2_11	R29
GPIO2_A1/CIF_D13/RGMII_TXEN/LCDC_D7	AR19	AVSS2_14	R31
GPIO0_A7/PCIE_WAKE_M0	AR21	DPHY_RX_D3N	R39
GPIO2_C0/CIF_D0/CLKOUT_ETHERNET	AR25	DDR_A6	T2
GPIO2_B7/CIF_CLKOUT/RGMII_CLK	AR27	DPHY_RX_D3P	T38
GPIO4_A6/SDMMC1_CMD	AR31	DDR_A1	U1
GPIO4_B7/UART4_RTS/SPI1_MISO_M0	AR33	VSS_54	U3
GPIO4_A7/SDMMC1_CLK	AR35	DDR_A5	U5
VSS_59	AR37	DDR_A2	U7
GPIO4_C1/I2C5_SCL	AR39	VSS_55	U9
PCIE_TX0N	AT2	DDR_VDD_3	U11
GPIO4_B2/SDMMC1_D2/UART1_CTS	AT38	VSS_56	U13

Pin name	Pin#	Pin name	Pin#
PCIE_TX0P	AU1	VSS_58	U15
AVSS1_5	AU3	LOGIC_VDD_2	U17
AVSS1_7	AU7	VSS_42	U19
GPIO0_B6/PCIE_PERST_M1	AU9	VSS_COM	U21
GPIO0_B1/I2C0_SDA	AU13	NPU_VDD_1	U23
GPIO0_B2/UART0_TX	AU15	VSS_65	U25
VSS_96	AU19	DPHY_RX_AVDD_0V8	U27
GPIO0_A1/TSADC_SHUT_M1	AU21	AVSS2_13	U29
GPIO2_A7/CIF_D5/RGMII_RXDV/SPI2_CSN_M1	AU25	ADC_IN1	U31
VSS_88	AU27	ADC_IN3	U33
GPIO2_B6/CIF_CLKIN/RGMII_RXD3	AU31	GPIO3_A2/I2S1_MCLK/PWM7	U35
VSS_87	AU33	AVSS2_10	U37
VSS_86	AU37	GPIO3_A0/I2S1_LRCK	U39
GPIO4_B6/UART4_CTS/SPI1_CSN0_M0	AU39	DDR_A3	V2
AVSS1_4	AV2	GPIO3_A1/I2S1_SCLK/PWM6	V38
PCIE_RX1N	AV4	DDR_A7	W1
OSC_24M_IN	AV6	VSS_62	W9
VSS_60	AV8	DDR_VDD_1	W11
GPIO0_B5/UART0_RTS/TEST_CLK1	AV10	VSS_63	W13
GPIO0_C1/I2C1_SDA	AV12	VSS_64	W15
GPIO0_B7/PWM0/OTG_DRV	AV14	LOGIC_VDD_3	W17
GPIO0_C5/PCIE_WAKE_M1/PWM2	AV16	VSS_71	W19
GPIO0_C3/PWM1/UART3_TX	AV18	NPU_VDD_COM	W21
GPIO0_A3/PCIE_CLKREQN_M0/SDMMC0_DETN	AV20	NPU_VDD_2	W23
GPIO0_A0/REF_CLKO	AV22	NPU_VDD_3	W25
OSC_BPASS	AV24	AVSS2_15	W27
GPIO2_A6/CIF_D4/RGMII_RXER/SPI2_MOSI_M1	AV26	VCCIO3	W29
GPIO2_B3/CIF_D9/RGMII_TXD3/LCDC_VSYNC_M0	AV28	ADC_IN0	W31
GPIO2_B4/CIF_VSYNC/RGMII_TXD2	AV30	ADC_IN2	W33
GPIO2_B5/CIF_HREF/RGMII_RXD2	AV32	GPIO3_A6/I2S0_SDI2/PDM_SDI2	W35
GPIO2_C7/LCDC_DEN	AV34	GPIO3_A3/I2S1_SDO/UART2_TX_M2	W37
GPIO2_D1/I2C3_SDA/UART2_RX_M1	AV36	GPIO3_A4/I2S1_SDI/UART2_RX_M2	W39
VSS_78	AV38	DDR_BA1	Y2
AVSS1_3	AW1	GPIO3_B0/I2S0_SCLK_RX/PDM_CLK0	Y38

2.6 Power/Ground IO Description

Table 2-2 Power/Ground IO information

Group	Ball#	Descriptions
VSS	A1 B2 C3 C7 C9 AW39 C13 C15 C19 C21 C25 B26 C33 J31 E3 G7 G13 G27 J3 L3 J9 J11 J13 J15 J17 J19 J21 J25 J27 J29 J33 L33 L7 L9 L11 L13 L15 L17 L19 L21 L23 U19 N9 R3 R9 R15 R19 R21 N23 N25 N27 R27 R25 U3 U9 U13 R13 U15 AR37 AV8 AJ27 W9 W13 W15 U25 AJ25 AE17 AA3 AL11 AA21 W19 AA19 AA27 R23 AC3 AC9 AG17 AV38 AC17 AC21 AC27 AA25 AG3 AG9 AJ1 AU37 AU33 AU27 AG19	Internal Core Ground, Digital IO Ground,

Group	Ball#	Descriptions
	AE21 AG21 AG23 AG25 AE25 AE27 AU19 AG27 AG29 AE37 AL37 AJ3 AJ7 U21	
AVSS1	AN3 AR3 AW1 AV2 AU3 AW5 AU7 AG13 AC13	Analog Ground
AVSS2	A39 B36 E33 E37 C37 G33 G37 L37 N37 U37 R29 N33 U29 R31	Analog Ground
OSC_VSS	AG15	OSC Ground
PLL_AVSS	AA13	PLL Analog Ground
DDR_AVSS	N11	DDR Analog Ground
OSC_VDD_1V8	AJ15	OSC IO Analog Power
PLL_AVDD_1V8	AA15	PLL Analog Power
PLL_AVDD_0V8	AC15	PLL Analog Power
PMU_VDD_0V8	AJ17	PMU Power Domain Power
PMUIO1_VDD_1V8	AJ19	PMUIO1 Power Domain Power
PMUIO2_VDD	AL15	PMUIO2 Power Domain Power
PPLL_AVDD_1V8	AJ11	PMU PLL Analog Power
PPLL_AVDD_0V8	AG11	PMU PLL Analog Power
DPHY_RX_AVDD_0V8	U27	DPHY RX 0.8V Analog Power
DPHY_RX_AVDD_1V8	L29	DPHY RX 1.8V Analog Power
DPHY_TX_AVDD_0V8	N29	DPHY TX 0.8V Analog Power
DPHY_TX_AVDD_1V8	L31	DPHY TX 1.8V Analog Power
PCIE_VDDREF_0V8	AJ13	PCIE REF Power
ADC_AVDD_1V8	N31	ADC Analog Power
USB_AVDD_1V8	AC11	U2B2.0 1.8V Analog Power
USB_AVDD_3V3	AE9	U2B2.0 3.3V Analog Power
USB_AVDD_0V8	AE11	U2B2.0 0.8V Analog Power
NPU_VDD	U23 W23 W25 AC25 AA23 AC23 AE23 W21	NPU Logic Power
ARM_VDD	AC19 AE19	ARM Core Power
LOGIC_VDD	R17 U17 W17 AA17	Logic Power
DDR_VDD	W11 R11 U11 N13 N15 N17 N19 N21	DDR PHY Power
PCIE_VCCA_1V8	AL13	PCIE Analog Power
PCIE_VCCA_0V8	AE15	PCIE Analog Power
PCIE_VCCD_0V8	AE13	PCIE Digital Power
VCCIO0	L27	VCCIO0 Power Domain Power
VCCIO1	AJ31	VCCIO1 Power Domain Power
VCCIO2	AJ23	VCCIO2 Power Domain Power
VCCIO3	W29	VCCIO3 Power Domain Power
VCCIO4	AA29	VCCIO4 Power Domain Power
VCCIO5	L25	VCCIO5 Power Domain Power
VCCIO6	AE31	VCCIO6 Power Domain Power
VCCIO7	AE29	VCCIO7 Power Domain Power

2.7 Function IO Description

Table 2-3 Function IO description

Pin#	Pin Name	Func1	Func2	Func3	Func4	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
AW23	NPOR	NPOR				I	I	2	fix up	PMUIO1
AV22	GPIO0_A0/REF_CLKO	GPIO0_A0	CLK_OUT_WIFI			I/O	I	4	down	
AU21	GPIO0_A1/TSADC_SHUT_M1	GPIO0_A1	TSADC_SHUTM1			I/O	I	2	z	
AN19	GPIO0_A2/PCIE_BUTTONRST	GPIO0_A2	PCIE_BUTTONRST			I/O	I	2	up	
AV20	GPIO0_A3/PCIE_CLKREQN_M0/SDMMC0_DETN	GPIO0_A3	SDMMC0_DETN	PCIE_CLKREQN_M0		I/O	I	2	up	
AW17	GPIO0_A4/PMIC_SLEEP	GPIO0_A4	PMIC_SLEEP			I/O	I	2	down	
AL17	GPIO0_A5/PCIE_PERST_M0	GPIO0_A5	PCIE_PRSTN_M0			I/O	I	2	up	
AW21	GPIO0_A6/TSADC_SHUT_M0/TSADC_SHUTORG	GPIO0_A6	TSADC_SHUTM0	TSADC_SHUTORG		I/O	I	2	z	
AR21	GPIO0_A7/PCIE_WAKE_M0	GPIO0_A7	PCIE_WAKE_M0			I/O	I	2	up	
AV24	OSC_BPASS	OSCBYPASS				I	I	2	up	
AW19	GPIO0_B0/I2C0_SCL	GPIO0_B0	I2C0_SCL			I/O	I	2	up	PMUIO2
AU13	GPIO0_B1/I2C0_SDA	GPIO0_B1	I2C0_SDA			I/O	I	2	up	
AU15	GPIO0_B2/UART0_TX	GPIO0_B2	UART0_TX	PMU_DEBUG0		I/O	I	2	down	
AW9	GPIO0_B3/UART0_RX	GPIO0_B3	UART0_RX	PMU_DEBUG1		I/O	I	2	down	
AR15	GPIO0_B4/UART0_CTS	GPIO0_B4	UART0_CTS	PMU_DEBUG2	PMU_DEBUG_SOUT	I/O	I	2	up	
AV10	GPIO0_B5/UART0_RTS/TEST_CLK1	GPIO0_B5	UART0_RTS	TEST_CLK1		I/O	I	2	up	
AU9	GPIO0_B6/PCIE_PERST_M1	GPIO0_B6	PCIE_PERST_M1L			I/O	I	2	up	
AV14	GPIO0_B7/PWM0/OTG_DRV	GPIO0_B7	PWM_0	OTG_DRV		I/O	I	2	down	
AN13	GPIO0_C0/I2C1_SCL	GPIO0_C0	I2C1_SCL		PMU_DEBUG5	I/O	I	2	down	
AV12	GPIO0_C1/I2C1_SDA	GPIO0_C1	I2C1_SDA			I/O	I	2	down	
AW13	GPIO0_C2/CLKIO_32K	GPIO0_C2	CLK_INOUT_32K			I/O	I	2	z	
AV18	GPIO0_C3/PWM1/UART3_TX	GPIO0_C3	PWM_1	UART3_TX	PMU_DEBUG3	I/O	I	2	down	
AW11	GPIO0_C4/PWM3/UART3_RX	GPIO0_C4	PWM_3	UART3_RX	PMU_DEBUG4	I/O	I	2	down	
AV16	GPIO0_C5/PCIE_WAKE_M1/PWM2	GPIO0_C5	PCIE_WAKE_M1	PWM_2		I/O	I	2	down	
AN15	GPIO0_C6/PCIE_CLKREQN_M1/UART3_CTS	GPIO0_C6	PCIE_CLKREQN_M1	UART3_CTS		I/O	I	2	down	
AR13	GPIO0_C7/UART3_RTS	GPIO0_C7		UART3_RTS		I/O	I	2	down	
AW15	DFTJTAG_TRSTN	DFTJTAGTRSTN				I/O	I	2	fix down	
AR9	DFTJTAG_TMS	DFTJTAGTMS				I/O	I	2	fix up	
E27	GPIO1_A0/EMMC_D0/SFC_SIO0	GPIO1_A0	EMMC_D0	SFC_SIO0		I/O	I	8	up	VCCIO0
B28	GPIO1_A1/EMMC_D1/SFC_SIO1	GPIO1_A1	EMMC_D1	SFC_SIO1		I/O	I	8	up	
A29	GPIO1_A2/EMMC_D2/SFC_SIO2	GPIO1_A2	EMMC_D2	SFC_SIO2		I/O	I	8	up	
B30	GPIO1_A3/EMMC_D3/SFC_SIO3	GPIO1_A3	EMMC_D3	SFC_SIO3		I/O	I	8	up	

Pin#	Pin Name	Func1	Func2	Func3	Func4	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
A31	GPIO1_A4/EMMC_D4/SFC_CSN0	GPIO1_A4	EMMC_D4	SFC_CSN0		I/O	I	8	up	
C31	GPIO1_A5/EMMC_D5/SFC_CLK	GPIO1_A5	EMMC_D5	SFC_CLK		I/O	I	8	up	
B32	GPIO1_A6/EMMC_D6/SPI2_MISO_M0	GPIO1_A6	EMMC_D6	SPI2M0_MISO		I/O	I	8	up	
A33	GPIO1_A7/EMMC_D7/SPI2_CLK_M0	GPIO1_A7	EMMC_D7	SPI2M0_CLK		I/O	I	8	up	
G31	GPIO1_B0/EMMC_PWREN/SPI2_MOSI_M0	GPIO1_B0	EMMC_PWREN	SPI2M0_MOSI		I/O	I	8	up	
E31	GPIO1_B1/EMMC_CLKOUT/SPI2_CSN_M0	GPIO1_B1	EMMC_CLKOUT	SPI2M0_CSN		I/O	I	8	up	
B34	GPIO1_B2/EMMC_CMD	GPIO1_B2	EMMC_CMD			I/O	I	8	up	
A35	GPIO1_B3/EMMC_RSTN	GPIO1_B3	EMMC_RSTN			I/O	I	8	down	
C27	GPIO1_B4/SPI0_MOSI/I2C2_SCL_M1/UART1_RX_M1	GPIO1_B4	SPI0_MOSI	I2C2M1_SCL	UART1_RXM1	I/O	I	4	up	VCCIO5
A27	GPIO1_B5/SPI0_MISO/I2C2_SDA_M1/UART1_TX_M1	GPIO1_B5	SPI0_MISO	I2C2M1_SDA	UART1_TXM1	I/O	I	4	up	
G25	GPIO1_B6/SPI0_CSN	GPIO1_B6	SPI0_CSN			I/O	I	4	up	
E25	GPIO1_B7/SPI0_CLK/PWM5	GPIO1_B7	SPI0_CLK	PWM_5		I/O	I	4	down	
AJ39	GPIO4_A0/SDMMC0_CMD/TEST_CLK0	GPIO4_A0	SDMMC0_CMD	TEST_CLK0		I/O	I	8	up	VCCIO6
AH38	GPIO4_A1/SDMMC0_CLK	GPIO4_A1	SDMMC0_CLK			I/O	I	8	down	
AG39	GPIO4_A2/SDMMC0_D0/UART2_TX_M0	GPIO4_A2	SDMMC0_D0	UART2_TXM0		I/O	I	8	up	
AE35	GPIO4_A3/SDMMC0_D1/UART2_RX_M0	GPIO4_A3	SDMMC0_D1	UART2_RXM0		I/O	I	8	up	
AF38	GPIO4_A4/SDMMC0_D2/JTAG_TCK	GPIO4_A4	SDMMC0_D2	JTAG_TCK		I/O	I	8	up	
AE33	GPIO4_A5/SDMMC0_D3/JTAG_TMS	GPIO4_A5	SDMMC0_D3	JTAG_TMS		I/O	I	8	up	
AR31	GPIO4_A6/SDMMC1_CMD	GPIO4_A6	SDMMC1_CMD			I/O	I	8	up	VCCIO1
AR35	GPIO4_A7/SDMMC1_CLK	GPIO4_A7	SDMMC1_CLK			I/O	I	8	down	
AN31	GPIO4_B0/SDMMC1_D0/UART1_RX_M0	GPIO4_B0	SDMMC1_D0	UART1_RXM0		I/O	I	8	up	
AP34	GPIO4_B1/SDMMC1_D1/UART1_TX_M0	GPIO4_B1	SDMMC1_D1	UART1_TXM0		I/O	I	8	up	
AT38	GPIO4_B2/SDMMC1_D2/UART1_CTS	GPIO4_B2	SDMMC1_D2	UART1_CTS		I/O	I	8	up	
AP38	GPIO4_B3/SDMMC1_D3/UART1_RTS	GPIO4_B3	SDMMC1_D3	UART1_RTS		I/O	I	8	up	
AN33	GPIO4_B4/UART4_RX/SPI1_CLK_M0	GPIO4_B4	UART4_RX	SPI1_CLK	PCIUSB_DEBUG0	I/O	I	4	up	
AJ29	GPIO4_B5/UART4_TX/SPI1_MOSI_M0	GPIO4_B5	UART4_TX	SPI1_MOSI	PCIUSB_DEBUG1	I/O	I	4	up	
AU39	GPIO4_B6/UART4_CTS/SPI1_CSN0_M0	GPIO4_B6	UART4_CTS	SPI1_CSN0	PCIUSB_DEBUG2	I/O	I	4	up	
AR33	GPIO4_B7/UART4_RTS/SPI1_MISO_M0	GPIO4_B7	UART4_RTS	SPI1_MISO	PCIUSB_DEBUG3	I/O	I	4	up	
AL33	GPIO4_C0/SPI1_CSN1_M0	GPIO4_C0		SPI1_CSN1	PCIUSB_DEBUG4	I/O	I	4	up	
AR39	GPIO4_C1/I2C5_SCL	GPIO4_C1	I2C5_SCL		PCIUSB_DEBUG5	I/O	I	4	up	
AL29	GPIO4_C2/I2C5_SDA	GPIO4_C2	I2C5_SDA		PCIUSB_DEBUG6	I/O	I	4	up	
AL27	GPIO4_C3	GPIO4_C3			PCIUSB_DEBUG7	I/O	I	4	up	
AL31	GPIO4_C4	GPIO4_C4				I/O	I	4	up	
AW25	GPIO2_A0/CIF_D12/RGMII_CRS/LCDC_D6	GPIO2_A0	CIF_D12	RGMII_CRS	LCDC_D6	I/O	I	4	down	
AR19	GPIO2_A1/CIF_D13/RGMII_TXEN/LCDC_D7	GPIO2_A1	CIF_D13	RGMII_TXEN	LCDC_D7	I/O	I	4	down	

Pin#	Pin Name	Func1	Func2	Func3	Func4	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
AL19	GPIO2_A2/CIF_D14/RGMII_TXD1/LCDC_D0	GPIO2_A2	CIF_D14	RGMII_TXD1	LCDC_D0	I/O	I	4	down	VCCIO2
AJ21	GPIO2_A3/CIF_D15/RGMII_TXD0/LCDC_D1	GPIO2_A3	CIF_D15	RGMII_TXD0	LCDC_D1	I/O	I	4	down	
AN21	GPIO2_A4/CIF_D2/RGMII_RXD0/SPI2_MISO_M1	GPIO2_A4	CIF_D2	RGMII_RXD0	SPI2M1_MISO	I/O	I	4	down	
AL21	GPIO2_A5/CIF_D3/RGMII_RXD1/SPI2_CLK_M1	GPIO2_A5	CIF_D3	RGMII_RXD1	SPI2M1_CLK	I/O	I	4	down	
AV26	GPIO2_A6/CIF_D4/RGMII_RXER/SPI2_MOSI_M1	GPIO2_A6	CIF_D4	RGMII_RXER	SPI2M1_MOSI	I/O	I	4	down	
AU25	GPIO2_A7/CIF_D5/RGMII_RXDV/SPI2_CSN_M1	GPIO2_A7	CIF_D5	RGMII_RXDV	SPI2M1_CSN	I/O	I	4	down	
AW29	GPIO2_B0/CIF_D6/RGMII_MDIO	GPIO2_B0	CIF_D6	RGMII_MDIO		I/O	I	4	down	
AW27	GPIO2_B1/CIF_D7/RGMII_COL	GPIO2_B1	CIF_D7	RGMII_COL		I/O	I	4	down	
AW31	GPIO2_B2/CIF_D8/RGMII_MDC/LCDC_HSYNC_M0	GPIO2_B2	CIF_D8	RGMII_MDC	LCDC_HSYNCM0	I/O	I	4	down	
AV28	GPIO2_B3/CIF_D9/RGMII_TXD3/LCDC_VSYNC_M0	GPIO2_B3	CIF_D9	RGMII_TXD3	LCDC_VSYNCM0	I/O	I	4	down	
AV30	GPIO2_B4/CIF_VSYNC/RGMII_TXD2	GPIO2_B4	CIF_VSYNC	RGMII_TXD2		I/O	I	4	down	
AV32	GPIO2_B5/CIF_HREF/RGMII_RXD2	GPIO2_B5	CIF_HREF	RGMII_RXD2		I/O	I	4	down	
AU31	GPIO2_B6/CIF_CLKIN/RGMII_RXD3	GPIO2_B6	CIF_CLKIN	RGMII_RXD3		I/O	I	4	down	
AR27	GPIO2_B7/CIF_CLKOUT/RGMII_CLK	GPIO2_B7	CIF_CLKOUT	RGMII_CLK		I/O	I	4	down	
AR25	GPIO2_C0/CIF_D0/CLKOUT_ETHERNET	GPIO2_C0	CIF_D0	CLK_OUT_ETHERNET		I/O	I	4	down	
AN27	GPIO2_C1/CIF_D1/RGMII_TXCLK	GPIO2_C1	CIF_D1	RGMII_TXCLK		I/O	I	4	down	
AN25	GPIO2_C2/CIF_D10/RGMII_RXCLK/LCDC_D2	GPIO2_C2	CIF_D10	RGMII_RXCLK	LCDC_D2	I/O	I	4	down	
AL23	GPIO2_C3/CIF_D11/LCDC_D3	GPIO2_C3	CIF_D11		LCDC_D3	I/O	I	4	down	
AL25	GPIO2_C4/LCDC_D4	GPIO2_C4			LCDC_D4	I/O	I	4	down	
AW35	GPIO2_C5/LCDC_D5	GPIO2_C5			LCDC_D5	I/O	I	4	down	
AW33	GPIO2_C6/LCDC_CLK	GPIO2_C6			LCDC_CLK	I/O	I	4	down	
AV34	GPIO2_C7/LCDC_DEN	GPIO2_C7			LCDC_DEN	I/O	I	4	down	
AW37	GPIO2_D0/I2C3_SCL/UART2_TX_M1	GPIO2_D0	I2C3_SCL	UART2_TXM1		I/O	I	2	up	
AV36	GPIO2_D1/I2C3_SDA/UART2_RX_M1	GPIO2_D1	I2C3_SDA	UART2_RXM1		I/O	I	2	up	
U39	GPIO3_A0/I2S1_LRCK	GPIO3_A0	I2S1_2CH_LRCK			I/O	I	4	down	VCCIO3
V38	GPIO3_A1/I2S1_SCLK/PWM6	GPIO3_A1	I2S1_2CH_SCLK	PWM_6		I/O	I	4	down	
U35	GPIO3_A2/I2S1_MCLK/PWM7	GPIO3_A2	I2S1_2CH_MCLK	PWM_7		I/O	I	4	down	
W37	GPIO3_A3/I2S1_SDO/UART2_TX_M2	GPIO3_A3	I2S1_2CH_SDO	UART2_TXM2		I/O	I	4	down	
W39	GPIO3_A4/I2S1_SDI/UART2_RX_M2	GPIO3_A4	I2S1_2CH_SDI	UART2_RXM2		I/O	I	4	down	
AA31	GPIO3_A5/I2S0_SDI3/PDM_SDI3	GPIO3_A5	I2S0_8CH_SDI3	PDM_SDI3		I/O	I	8	down	VCCIO4
W35	GPIO3_A6/I2S0_SDI2/PDM_SDI2	GPIO3_A6	I2S0_8CH_SDI2	PDM_SDI2		I/O	I	8	down	
AC29	GPIO3_A7/I2S0_SDI1/PDM_SDI1	GPIO3_A7	I2S0_8CH_SDI1	PDM_SDI1		I/O	I	8	down	
Y38	GPIO3_B0/I2S0_SCLK_RX/PDM_CLK0	GPIO3_B0	I2S0_8CH_SCLKRX	PDM_CLK0		I/O	I	8	down	
AB38	GPIO3_B1/I2S0_LRCK_RX/PDM_CLK1	GPIO3_B1	I2S0_8CH_LRCKRX	PDM_CLK1		I/O	I	8	down	
AC33	GPIO3_B2/I2S0_SDO3/ISP_FLASHTRIGIN/LCDC_HSYNC_M1	GPIO3_B2	I2S0_8CH_SDO3	ISP_FLASHTRIGIN	LCDC_HSYNCM1	I/O	I	8	down	

Pin#	Pin Name	Func1	Func2	Func3	Func4	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
AC31	GPIO3_B3/I2S0_SDO2/I2C2_SCL_M0/LCDC_VSYNC_M1	GPIO3_B3	I2S0_8CH_SDO2	I2C2M0_SCL	LCDC_VSYNCM1	I/O	I	8	down	
AC35	GPIO3_B4/I2S0_SDO1/I2C2_SDA_M0	GPIO3_B4	I2S0_8CH_SDO1	I2C2M0_SDA		I/O	I	8	down	
AC39	GPIO3_B5/I2S0_MCLK/ISP_SHUTTEREN	GPIO3_B5	I2S0_8CH_MCLK	ISP_SHUTTEREN		I/O	I	8	down	
AE39	GPIO3_B6/I2S0_LRCK_TX/ISP_FLASHTRIGOUT	GPIO3_B6	I2S0_8CH_LRCKTX	ISP_FLASHTRIGOUT		I/O	I	8	down	
AD38	GPIO3_B7/I2S0_SCLK_TX/ISP_PRELIGHTTRIG	GPIO3_B7	I2S0_8CH_SCLKTX	ISP_PRELIGHTTRIG		I/O	I	8	down	
AC37	GPIO3_C0/I2S0_SDO0/ISP_SHUTTERTRIG	GPIO3_C0	I2S0_8CH_SDO0	ISP_SHUTTERTRIG		I/O	I	8	down	
AA39	GPIO3_C1/I2S0_SDI0/PDM_SDI0	GPIO3_C1	I2S0_8CH_SDI0	PDM_SDI0		I/O	I	8	down	
AN37	GPIO3_C2/LCDC_D8/UART5_TX/I2C4_SCL	GPIO3_C2	LCDC_D8	UART5_TX	I2C4_SCL	I/O	I	8	down	VCCIO7
AM38	GPIO3_C3/LCDC_D9/UART5_RX/I2C4_SDA	GPIO3_C3	LCDC_D9	UART5_RX	I2C4_SDA	I/O	I	8	down	
AL39	GPIO3_C4/LCDC_D10/UART6_TX	GPIO3_C4	LCDC_D10	UART6_TX		I/O	I	8	down	
AJ33	GPIO3_C5/LCDC_D11/UART6_RX	GPIO3_C5	LCDC_D11	UART6_RX		I/O	I	8	down	
AN39	GPIO3_C6/LCDC_D12/UART7_TX	GPIO3_C6	LCDC_D12	UART7_TX		I/O	I	8	down	
AL35	GPIO3_C7/LCDC_D13/UART7_RX/SPI1_CLK_M1	GPIO3_C7	LCDC_D13	UART7_RX	SPI1M1_CLK	I/O	I	8	down	
AJ35	GPIO3_D0/LCDC_D14/PWM8/SPI1_MOSI_M1	GPIO3_D0	LCDC_D14	PWM_8	SPI1M1_MOSI	I/O	I	8	down	
AG31	GPIO3_D1/LCDC_D15/PWM9/SPI1_CSN0_M1	GPIO3_D1	LCDC_D15	PWM_9	SPI1M1_CSN0	I/O	I	8	down	
AK38	GPIO3_D2/LCDC_D16/PWM10/SPI1_MISO_M1	GPIO3_D2	LCDC_D16	PWM_10	SPI1M1_MISO	I/O	I	8	down	
AJ37	GPIO3_D3/LCDC_D17/PWM11/SPI1_CSN1_M1	GPIO3_D3	LCDC_D17	PWM_11	SPI1M1_CSN1	I/O	I	8	down	
L39	DPHY_RX_CLKN	DPHY_RX_CLKN				A			NA	
M38	DPHY_RX_CLKP	DPHY_RX_CLKP				A			NA	
L35	DPHY_RX_D0N	DPHY_RX_D0N				A			NA	
J39	DPHY_RX_D1N	DPHY_RX_D1N				A			NA	
N39	DPHY_RX_D2N	DPHY_RX_D2N				A			NA	
R39	DPHY_RX_D3N	DPHY_RX_D3N				A			NA	
N35	DPHY_RX_D0P	DPHY_RX_D0P				A			NA	
K38	DPHY_RX_D1P	DPHY_RX_D1P				A			NA	
P38	DPHY_RX_D2P	DPHY_RX_D2P				A			NA	
T38	DPHY_RX_D3P	DPHY_RX_D3P				A			NA	
E35	DPHY_TX_CLKN	DPHY_TX_CLKN				A			NA	
G35	DPHY_TX_CLKP	DPHY_TX_CLKP				A			NA	
B38	DPHY_TX_D0N	DPHY_TX_D0N				A			NA	
C39	DPHY_TX_D1N	DPHY_TX_D1N				A			NA	
E39	DPHY_TX_D2N	DPHY_TX_D2N				A			NA	
G39	DPHY_TX_D3N	DPHY_TX_D3N				A			NA	
A37	DPHY_TX_D0P	DPHY_TX_D0P				A			NA	
D38	DPHY_TX_D1P	DPHY_TX_D1P				A			NA	

Pin#	Pin Name	Func1	Func2	Func3	Func4	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
F38	DPHY_TX_D2P	DPHY_TX_D2P				A			NA	
H38	DPHY_TX_D3P	DPHY_TX_D3P				A			NA	
E5	DDR_DM0	DDR_DM0				A			NA	
H2	DDR_DM1	DDR_DM1				A			NA	
A5	DDR_DQ0	DDR_DQ0				A			NA	
F6	DDR_DQ1	DDR_DQ1				A			NA	
F2	DDR_DQ10	DDR_DQ10				A			NA	
E1	DDR_DQ11	DDR_DQ11				A			NA	
D2	DDR_DQ12	DDR_DQ12				A			NA	
C1	DDR_DQ13	DDR_DQ13				A			NA	
B4	DDR_DQ14	DDR_DQ14				A			NA	
A3	DDR_DQ15	DDR_DQ15				A			NA	
B6	DDR_DQ2	DDR_DQ2				A			NA	
E7	DDR_DQ3	DDR_DQ3				A			NA	
B8	DDR_DQ4	DDR_DQ4				A			NA	
A7	DDR_DQ5	DDR_DQ5				A			NA	
B10	DDR_DQ6	DDR_DQ6				A			NA	
A9	DDR_DQ7	DDR_DQ7				A			NA	
G1	DDR_DQ8	DDR_DQ8				A			NA	
L5	DDR_DQ9	DDR_DQ9				A			NA	
G9	DDR_DQS0P	DDR_DQS0P				A			NA	
J7	DDR_DQS1P	DDR_DQS1P				A			NA	
E9	DDR_DQS0N	DDR_DQS0N				A			NA	
J5	DDR_DQS1N	DDR_DQS1N				A			NA	
R1	LPDDR3_A0/DDR3_A9	LPDDR3_A0	DDR3_A9			A			NA	
U1	LPDDR3_A1/DDR3_A14	LPDDR3_A1	DDR3_A14			A			NA	
AD2	DDR3_A0		DDR3_A0			A			NA	
R7	DDR3_A7		DDR3_A7			A			NA	
AB2	DDR3_CASB		DDR3_CASB			A			NA	
AH2	DDR3_A8		DDR3_A8			A			NA	
AG5	DDR3_ODT0		DDR3_ODT0			A			NA	
AE1	DDR3_BA1		DDR3_BA1			A			NA	
AF2	DDR3_RASB		DDR3_RASB			A			NA	
AG7						A			NA	
U7	LPDDR3_A2/DDR3_A13	LPDDR3_A2	DDR3_A13			A			NA	

Pin#	Pin Name	Func1	Func2	Func3	Func4	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
V2	LPDDR3_A3/DDR3_A11	LPDDR3_A3	DDR3_A11			A			NA	
AA5	LPDDR3_A4/DDR3_A2	LPDDR3_A4	DDR3_A2			A			NA	
U5	LPDDR3_A5/DDR3_A4	LPDDR3_A5	DDR3_A4			A			NA	
T2	LPDDR3_A6/DDR3_A3	LPDDR3_A6	DDR3_A3			A			NA	
W1	LPDDR3_A7/DDR3_A6	LPDDR3_A7	DDR3_A6			A			NA	
P2	LPDDR3_A8/DDR3_A5	LPDDR3_A8	DDR3_A5			A			NA	
AC7	LPDDR3_A9/DDR3_A1	LPDDR3_A9	DDR3_A1			A			NA	
N1	DDR3_CSB0		DDR3_CSB0			A			NA	
E13	DDR_DM2	DDR_DM2				A			NA	
E19	DDR_DM3	DDR_DM3				A			NA	
B12	DDR_DQ16	DDR_DQ16				A			NA	
A11	DDR_DQ17	DDR_DQ17				A			NA	
B20	DDR_DQ26	DDR_DQ26				A			NA	
A21	DDR_DQ27	DDR_DQ27				A			NA	
A23	DDR_DQ28	DDR_DQ28				A			NA	
B22	DDR_DQ29	DDR_DQ29				A			NA	
A25	DDR_DQ30	DDR_DQ30				A			NA	
B24	DDR_DQ31	DDR_DQ31				A			NA	
A13	DDR_DQ18	DDR_DQ18				A			NA	
G19	DDR_DQ19	DDR_DQ19				A			NA	
A15	DDR_DQ20	DDR_DQ20				A			NA	
B14	DDR_DQ21	DDR_DQ21				A			NA	
A17	DDR_DQ22	DDR_DQ22				A			NA	
B16	DDR_DQ23	DDR_DQ23				A			NA	
A19	DDR_DQ24	DDR_DQ24				A			NA	
B18	DDR_DQ25	DDR_DQ25				A			NA	
G15	DDR_DQS2P	DDR_DQS2P				A			NA	
G21	DDR_DQS3P	DDR_DQS3P				A			NA	
E15	DDR_DQS2N	DDR_DQS2N				A			NA	
E21	DDR_DQS3N	DDR_DQS3N				A			NA	
R5	LPDDR3_BA0/DDR3_BA2	LPDDR3_BA0	DDR3_BA2			A			NA	
Y2	LPDDR3_BA1/DDR3_A12	LPDDR3_BA1	DDR3_A12			A			NA	
K2	DDR3_BA0		DDR3_BA0			A			NA	
AA7	DDR3_WEB		DDR3_WEB			A			NA	
L1	LPDDR3_CK/DDR3_CK	LPDDR3_CK	DDR3_CK			A			NA	

Pin#	Pin Name	Func1	Func2	Func3	Func4	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
M2	LPDDR3_CKB/DDR3_CKB	LPDDR3_CKB/	DDR3_CKB			A			NA	
AC5	LPDDR3_CKE/DDR3_CKE	LPDDR3_CKE	DDR3_CKE			A			NA	
AC1	LPDDR3_CSB0/DDR3_A10	LPDDR3_CSB0	DDR3_A10			A			NA	
AJ5	LPDDR3_CSB1/DDR3_CSB1	LPDDR3_CSB1	DDR3_CSB1			A			NA	
AA1	LPDDR3_ODT0/DDR3_A15	LPDDR3_ODT0	DDR3_A15			A			NA	
AG1	LPDDR3_ODT1/DDR3_ODT1	LPDDR3_ODT1	DDR3_ODT1			A			NA	
AA15	PLL_AVDD_1V8	PLL_AVDD_1V8				A			NA	
J23	DDR_VERFO	DDR_VERFO				A			NA	
J1	DDR_RESETN	DDR_RESETN				A			NA	
AA9	DDR_RZQ	DDR_RZQ				A			NA	
AN7	PCIE_REFCLKN	PCIE_REFCLKN				A			NA	
AN5	PCIE_REFCLKP	PCIE_REFCLKP				A			NA	
AN9	PCIE_RBIAS	PCIE_RBIAS				A			NA	
AP2	PCIE_RX0N/USB3_SSRXN	PCIE_RX0N	USB3_SSRXN			A			NA	
AV4	PCIE_RX1N	PCIE_RX1N				A			NA	
AR1	PCIE_RX0P/USB3_SSRXP	PCIE_RX0P	USB3_SSRXP			A			NA	
AW3	PCIE_RX1P	PCIE_RX1P				A			NA	
AT2	PCIE_TX0N/USB3_SSTXN	PCIE_TX0N	USB3_SSTXN			A			NA	
AR7	PCIE_TX1N	PCIE_TX1N				A			NA	
AU1	PCIE_TX0P/USB3_SSTXP	PCIE_TX0P	USB3_SSTXP			A			NA	
AR5	PCIE_TX1P	PCIE_TX1P				A			NA	
W31	ADC_IN0	ADC_IN0				A			NA	
U31	ADC_IN1	ADC_IN1				A			NA	
W33	ADC_IN2	ADC_IN2				A			NA	
U33	ADC_IN3	ADC_IN3				A			NA	
AJ9	USB_OTG_ID	USB_OTG_ID				A			NA	
AK2	USB_OTG_DM	USB_OTG_DM				A			NA	
AL1	USB_OTG_DP	USB_OTG_DP				A			NA	
AM2	USB_HOST_DM	USB_HOST_DM				A			NA	
AN1	USB_HOST_DP	USB_HOST_DP				A			NA	
AL9	USB_OTG_VBUS	USB_OTG_VBUS				A			NA	
AV6	OSC_24M_IN	OSC_24M_IN				A			NA	
AW7	OSC_24M_OUT	OSC_24M_OUT				A			NA	

Notes:

①:Type: I = input, O = output, I/O = input/output (bidirectional), A = Analog

②:Output Drive Unit is mA, only Digital IO has driver strength value;

③:Def: I = input without any pull resistor, O = output without any pull resistor;

④:INT: interrupt

2.8 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 IO function description list

Interface	Pin Name	Direction	Description
Misc	OSC_24M_IN	I	Clock input of 24MHz crystal
	OSC_24M_OUT	O	Clock output of 24MHz crystal
	NPOR	I	Chip hardware reset

Interface	Pin Name	Direction	Description
SWJ-DP	JTAG_TCK	I	JTAG interface clock input/SWD interface clock input
	JTAG_TMS	I/O	JTAG interface TMS input/SWD interface data out

Interface	Pin Name	Direction	Description
SDMMC Host Controller	SDMMC0_CLK	O	sdmmc card clock
	SDMMC0_CMD	I/O	sdmmc card command output and response input
	SDMMC0_D*i* (*i*=0~3)	I/O	sdmmc card data input and output
	SDMMC0_DETN	I	sdmmc card detect signal, 0 represents presence of card

Interface	Pin Name	Direction	Description
SDIO Host Controller	SDMMC1_CLK	O	sdio card clock
	SDMMC1_CMD	I/O	sdio card command output and response input
	SDMMC1_D*i* (*i*=0~3)	I/O	sdio card data input and output

Interface	Pin Name	Direction	Description
eMMC Interface	EMMC_CLKOUT	O	emmc card clock
	EMMC_CMD	I/O	emmc card command output and response input
	EMMC_D*i* (*i*=0~7)	I/O	emmc card data input and output

Interface	Pin Name	Direction	Description
SFC Controller	SFC_CLK	I/O	sfc serial clock
	SFC_CSNx*(x=0)*	I/O	sfc chip select signal,low active
	SFC_SIOx*(x=0,3)*	O	sfc serial data output

Interface	Pin Name	Direction	Description
LCDC	LCDC_DCLK	O	LCDC RGB interface display clock out, MCU i80 interface RS signal
	LCDC_VSYNC	O	LCDC RGB interface vertical sync pulse, MCU i80 interface CSN signal
	LDCD_HSYNC	O	LCDC RGB interface horizontal sync pulse, MCU i80 interface WEN signal

Interface	Pin Name	Direction	Description
	LCDC_DEN	O	LCDC RGB interface data enable, MCU i80 interface REN signal
	LCDC_D*i* (*i*=0~17)	O	LCDC data output/input

Interface	Pin Name	Direction	Description
DDR Interface	CLKP	O	Active-high clock signal
	CLKN	O	Active-low clock signal
	CKE	O	Active-high clock enable signal
	CSNi (i=0,1)	O	Active-low chip select signal .There are two chip select
	RASn	O	Active-low row address strobe
	CASn	O	Active-low column address strobe
	WEn	O	Active-low write enable strobe
	BAi(i=0,1,2)	O	Bank address signal
	Ai(i=0~15)	O	Address signal
	DQi(i=0~31)	I/O	Bidirectional data line
	DQS[*i*]_P (i=0~3)	I/O	Active-high bidirectional data strobes
	DQS*i*_N (i=0~3)	I/O	Active-low bidirectional data strobes
	DMi (i=0~3)	O	Active-low data mask signal
	ODTi (i=0,1)	O	On-Die Termination output signal for two chip select.
	RESETn	O	DDR3/DDR4 reset signal

Interface	Pin Name	Direction	Description
I2S0/PCM Controller	I2S0_8CH_MCLK	O	I2S/PCM clock to external device
	I2S0_8CH_SCLK	I/O	I2S/PCM serial clock
	I2S0_8CH_LRCKRX	I/O	I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S0_8CH_LRCKTX	I/O	I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S0_8CH_SDI*i* (*i*=1~3)	I	I2S/PCM serial data input
	I2S0_8CH_SDO*i* (*i*=1~3)	O	I2S/PCM serial data output

Interface	Pin Name	Direction	Description
I2S1/PCM Controller	I2S1_2CH_MCLK	O	I2S/PCM clock source
	I2S1_2CH_SCLK	I/O	I2S/PCM serial clock
	I2S1_2CH_LRCKRX	I/O	I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S1_2CH_LRCKTX	I/O	I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S1_2CH_SDI	I	I2S/PCM serial data input
	I2S1_2CH_SDO	O	I2S/PCM serial data output

Interface	Pin Name	Direction	Description
PDM	PDM_CLK	O	PDM serial clock
	PDM_SDI*i* (*i*=0~3)	I	PDM data

Interface	Pin Name	Direction	Description
SPI0	SPI0_CLK	I/O	SPI serial clock
	SPI0_CSN*i* (*i*=0)	I/O	SPI chip select signal, low active
	SPI0_TXD	O	SPI serial data output
	SPI0_RXD	I	SPI serial data input

Interface	Pin Name	Direction	Description
SPI1	SPI1_CLK	I/O	SPI serial clock
	SPI1_CSN*i* (*i*=0,1)	I/O	SPI chip select signal, low active
	SPI1_TXD	O	SPI serial data output
	SPI1_RXD	I	SPI serial data input

Interface	Pin Name	Direction	Description
SPI2	SPI2_CLK	I/O	SPI serial clock
	SPI2_CSN*i* (*i*=0,1)	I/O	SPI chip select signal, low active
	SPI2_TXD	O	SPI serial data output
	SPI2_RXD	I	SPI serial data input

Interface	Pin Name	Direction	Description
PWM	PWM0	I/O	Pulse Width Modulation input or output
	PWM1	I/O	Pulse Width Modulation input or output
	PWM2	I/O	Pulse Width Modulation input or output
	PWM3	I/O	Pulse Width Modulation input or output, used for IR application recommended
	PWM5	I/O	Pulse Width Modulation input and output
	PWM6	I/O	Pulse Width Modulation input or output
	PWM7	I/O	Pulse Width Modulation input or output, used for IR application recommended
	PWM8	I/O	Pulse Width Modulation input or output
	PWM9	I/O	Pulse Width Modulation input or output
	PWM10	I/O	Pulse Width Modulation input or output
	PWM11	I/O	Pulse Width Modulation input or output, used for IR application recommended

Interface	Pin Name	Direction	Description
I2C	I2C*i*_SDA (*i*=0,1,2,3,4,5)	I/O	I2C data
	I2C*i*_SCL (*i*=0,1,2,3,4,5)	I/O	I2C clock

Interface	Pin Name	Direction	Description
UART	UART*i*_RX (*i*=0,1,2,3,4,5)	I	UART serial data input
	UART*i*_TX (*i*=0,1,2,3,4,5)	O	UART serial data output
	UART*i*_CTS (*i*=0,1,3,4,5)	I	UART clear to send modem status input
	UART*i*_RTS (*i*=0,1,3,4,5)	O	UART modem control request to send output

Interface	Pin Name	Direction	Description
GMAC	RGMII_CLK	I/O	MAC REC_CLK output or external clock input
	RGMII_TXCLK	O	MAC TX clock
	RGMII_RXCLK	I	MAC RX clock
	RGMII_RXDV	I	MAC RX control
	RGMII_MDC	O	MAC management interface clock
	RGMII_MDIO	I/O	MAC management interface data
	RGMII_TXD*i*(*i*=0~3)	O	MAC TX data
	RGMII_RXD*i*(*i*=0~3)	I	MAC RX data
	RGMII_TXEN	O	MAC TX data enable
	RGMII_RXER	I	MAC RX error signal
	RGMII_RXDV	O	MAC RX enable
	RGMII_CRS	I	PHY CRS signal
	RGMII_COL	I	PHY collision detected

Interface	Pin Name	Direction	Description
USB 2.0	USB_HOST_DP	I/O	USB 2.0 Data signal DP
	USB_HOST_DM	I/O	USB 2.0 Data signal DM
	USB_OTG_DP	I/O	USB 2.0 Data signal DP
	USB_OTG_DM	I/O	USB 2.0 Data signal DM
	USB_RBIAS	I/O	Connect 133 ohm resistor to ground to generate reference current
	USB_VBUS	I	Insert detect when act as USB device
	USB_ID	I	USB Mini-Receptacle Identifier

Interface	Pin Name	Direction	Description
PCIe/USB3	PCIE_RX0P/USB3_SSRXP	I	Channel 0 positive serial input
	PCIE_RX0N/USB3_SSRXN	I	Channel 0 negative serial input
	PCIE_RX1P	I	Channel 1 positive serial input
	PCIE_RX1N	I	Channel 1 negative serial input
	PCIE_TX0P/USB3_SSTXP	O	Channel 0 positive serial output
	PCIE_TX0N/USB3_SSTXN	O	Channel 0 negative serial output
	PCIE_TX1P	O	Channel 1 positive serial output
	PCIE_TX1N	O	Channel 1 negative serial output
	PCIE_REFCLKP	I/O	Low-swing differential clock pair
	PCIE_REFCLKN	I/O	Low-swing differential clock pair

Interface	Pin Name	Direction	Description
	PCIE_RBIAS	I	2Kohm external resistance bias to ground

Interface	Pin Name	Direction	Description
Camera IF	CIF_D*i*(*i*=0~15)	I	Camera interface input pixel data
	CIF_VSYNC	I	Camera interface vertical sync signal
	CIF_CLKIN	I	Camera interface input pixel clock
	CIF_HREF	I	Camera interface horizontial sync signal

Interface	Pin Name	Direction	Description
MIPI_DSI	MIPI_TX_D*i*N(*i*=0~3)	O	MIPI DSI negative differential data line transceiver output
	MIPI_TX_D*i*P(*i*=0~3)	O	MIPI DSI positive differential data line transceiver output
	MIPI_TX_CLKP	O	MIPI DSI positive differential clock line transceiver output
	MIPI_TX_CLKN	O	MIPI DSI negative differential clock line transceiver output

Interface	Pin Name	Direction	Description
MIPI_CSI	MIPI_CSI_DN*i*(*i*=0~3)	I	MIPI CSI negative differential data line transceiver output
	MIPI_CSI_DP*i*(*i*=0~3)	I	MIPI CSI positive differential data line transceiver output
	MIPI_CSI_CLKP	I	MIPI CSI positive differential clock line transceiver output
	MIPI_CSI_CLKN	I	MIPI CSI negative differential clock line transceiver output
	MIPI_CSI_RBIAS	I	MIPI CSI external resistor connection, connect 2K ohm resistor to ground

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for CPU	CORE_VDD	0	1.045	V
Supply voltage for NPU	NPU_VDD	0	1.045	V
Supply voltage for Logic	LOGIC_VDD	0	0.98	V
Supply voltage for PMU	PMU_VDD	0	0.98	V
0.8V supply voltage		0	0.98	V
1.8V supply voltage		0	1.98	V
3.3V supply voltage		0	3.63	V
Supply voltage for DDR IO		0	TBD	V
Storage Temperature	Tstg	TBD	TBD	℃
Max Conjunction Temperature	Tj	NA	125	℃

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Symbol	Min	Typ	Max	Unit
Voltage for CPU	CORE_VDD	0.72	0.80	0.945	V
Voltage for NPU	NPU_VDD	0.72	0.80	0.945	V
Voltage for Logic	LOGIC_VDD	0.72	0.80	0.88	V
Voltage for PMU	PMU_VDD	0.72	0.80	0.88	V
Digital GPIO Power (1.8V)	PMUIO1	1.62	1.80	1.98	V
Digital GPIO Power (3.3V/1.8V)	VCCIO0,VCCIO1,VCCIO2, VCCIO3,VCCIO4,VCCIO5, VCCIO6,VCCIO7,PMUIO2	2.97 1.62	3.30 1.80	3.63 1.98	V
LPDDR3 IO power	DDR_VDD	1.14	1.20	1.32	V
DDR3 IO power	DDR_VDD	1.425	1.50	1.575	V
DDR3L IO Power	DDR_VDD	1.283	1.35	1.418	V
LPDDR2 IO Power	DDR_VDD	1.14	1.20	1.26	V
eFUSE Analog Power	EFUSE_VQPS	1.62	1.80	1.98	V
PLL Analog Power(0.8V)	PLL_AVDD_0V8	0.72	0.80	0.88	V
PLL Analog Power(1.8V)	PLL_AVDD_1V8	1.62	1.80	1.98	V
SARADC Analog Power	SADC_AVDD_1V8	1.62	1.80	1.98	V
USB 2.0 OTG/Host Analog Power (0.8V)	USB_VDD_0V8	0.72	0.80	0.88	V
USB 2.0 OTG/Host Analog Power (1.8V)	USB_AVDD_1V8	1.62	1.80	1.98	V
USB 2.0 OTG/Host Analog Power (3.3V)	USB_AVDD_3V3	2.97	3.30	3.63	V
PCIe Power (0.8V)	PCIE_VCCATX, PCIE_VCCD, PCIE_VDDREF,PCIE_VDD	0.72	0.80	0.88	V
PCIe Analog Power(1.8V)	PCIE_VCCA_1V8	1.62	1.80	1.98	V
DPHY Power(0.8V)	DPHY_VCCA_0V8,DPHY_VDD	0.72	0.80	0.88	V
DPHY Analog Power(1.8V)	DPHY_VCCA_1V8	1.62	1.80	1.98	V
OSC input clock frequency		NA	24	NA	MHz
Max CPU frequency of A35		NA	NA	TBD	GHz
Ambient Operating Temperature	T_A	TBD	25	TBD	℃

Notes:

① ***Symbol name is same as the pin name in the io descriptions***

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	NA	0.325*VCC	V
	Input High Voltage	Vih	0.7*VCC	NA	VCC+0.3	V
	Output Low Voltage	Vol	NA	NA	0.2*VCC	V
	Output High Voltage	Voh	0.8*VCC	NA	NA	V
	Pullup Resistor	Rpu	35	60	100	Kohm
	Pulldown Resistor	Rpd	35	60	110	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	0	VCC*0.35	V
	Input High Voltage	Vih	0.7*VCC	VCC	VCC + 0.3	V
	Output Low Voltage	Vol	NA	NA	0.4	V
	Output High Voltage	Voh	VCC-0.4	NA	NA	V
	Pull-up Resistor	Rpu	35	63	120	Kohm
	Pull-down Resistor	Rpd	35	61	114	Kohm

Parameters		Symbol	Min	Typ	Max	Unit
DDR IO @ LPDDR2 mode	Input High Voltage	Vih_ddr	VREF + 0.13	NA	DDR_VDD	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.13	V
	Output High Voltage	Voh_ddr	VREF + 0.13	NA	DDR_VDD	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF-0.13	V
DDR IO @ LPDDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.1	NA	DDR_VDD	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.1	V
	Output High Voltage	Voh_ddr	VREF + 0.1	NA	DDR_VDD	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.1	V
DDR IO @ @DDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.1	NA	DDR_VDD	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.10	V
	Output High Voltage	Voh_ddr	VREF + 0.1	NA	DDR_VDD	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.10	V
DDR IO @ @DDR3L mode	Input High Voltage	Vih_ddr	VREF + 0.1	NA	DDR_VDD	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.09	V
	Output High Voltage	Voh_ddr	VREF + 0.1	NA	DDR_VDD	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.1	V

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 3.3V, pull down disabled	NA	NA	10	uA
			Vin = 3.3V, pull down enabled	NA	NA	106.4	uA
	Low level input current	Iil	Vin = 0V, pull up disabled	NA	NA	10	uA
			Vin = 0V, pull up enabled	NA	NA	107.8	uA
Digital GPIO	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
@1.8V	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 1.8V, pull down disabled	NA	NA	10	uA
			Vin = 1.8V, pull down enabled	NA	NA	61.3	uA
	Low level input current	Iil	Vin = 0V, pull up disabled	NA	NA	10	uA
			Vin = 0V, pull up enabled	NA	NA	61.4	uA

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
PLL	Input clock frequency(Int)	F_{in}	Fin = FREF @1.8V/0.8V	2	NA	1250	MHz
	Input clock frequency(Frac)	F_{in}	Fin = FREF @1.8V/0.8V	10	NA	1250	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @1.8V/0.8V	1250	NA	5000	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @1.8V/0.8V	25	NA	5000	MHz
	Lock time	T_{lt}	FREF=24M,REFDIV=1 @1.8V/0.8V	NA	500	1000	Input clock cycles
	VDDHV current consumption		Fvco = 1250MHz, @1.8V ***Current scale as (Fvco/1GHz)$^{1.5}$***	NA	0.7	0.9	mA
	VDD Current consumption		VDD =0.8V	NA	0.05	0.1	uA/MHz
	Power consumption (power-down mode)		PD=HIGH, @27 ℃	NA	25	NA	uA

Notes:

① *REFDIV is the input divider value;*
② *FBDIV is the feedback divider value;*
③ *POSTDIV is the output divider value.*

3.6 Electrical Characteristics for USB 2.0 Interface

Table 3-6 Electrical Characteristics for USB 2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
Output resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40	45	50	ohms
		HS mode (Vout = 0 to 800mV)	40	45	50	ohms
Output Capacitance	COUT	seen from D+ or D-	NA	NA	3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	2.7	NA	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
High input level	VIH		0.6	0.8	NA	V
Low input level	VIL		NA	0	0.2	V
Receiver sensitivity	RSENS	Classic mode	NA	+-250	NA	mV
		HS mode	NA	+-25	NA	mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and	0.1	0.2	0.3	V

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
		squelch comparator)				
		HS mode (disconnect comparator)	0.5	0.6	0.7	V
Input capacitance		(seen at D+ or D-)	NA	NA	3	pF
Squelch threshold			100	112	150	mV
Disconnect threshold			570	590	625	mV
High output level	VOH		2.8	3.3	NA	V
Low output level	VOL		NA	0	0.3	V

3.7 Electrical Characteristics for DDR IO

Table 3-7 Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
DDR IO @DDR3 mode	Input leakage current, SSTL mode, unterminated		@ 1.5V , 125℃	NA	0	NA	uA
DDR IO @DDR3L mode	Input leakage current		@ 1.35V , 125℃	NA	0	NA	nA
DDR IO @LPDDR2/LPDDR3 mode	Input leakage current		@ 1.2V , 125℃	NA	0	0.49	nA
DDR IO @DDR4 mode	Input leakage current		@ 1.2V , 125℃	-5	0	+5	uA

3.8 Electrical Characteristics for TSADC

Table 3-8 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Temperature Resolution			NA	+/-5	NA	℃
Temperature Range			-40		125	℃
Analog power	IAVDD	Fs= 50KS/s	NA	240	NA	uA
Digital power	IVDD	Fs= 50KS/s	NA	10	NA	uA
Clock Frequency	Fclk	Fclk	NA		800	KHz
Power Down Current from Analog	IAVDD	Power down	NA	1	NA	uA
Power Down Current from Digital	IVDD	Power down	NA	1	NA	uA

3.9 Electrical Characteristics for SARADC

Table 3-9 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Resolution			NA	10	NA	bit
Effective Number of Bit	ENOB		NA	9	NA	bit
Differential Nonlinearity	DNL		-1	NA	+1	LSB
Integral Nonlinearity	INL		-2	NA	+2	LSB
Input Voltage Range	VIN		0	NA	1	AVDD
Input Capacitance	CIN		NA	8	NA	pF
Sampling Rate	fs		NA	NA	1	MS/s
Analog power	IAVDD	Fs= 1MS/s	NA	700	NA	uA
Digital power	IVDD	Fs= 1MS/s	NA	50	NA	uA

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Power Down Current from Analog	IAVDD	Power down	NA	1	NA	uA
Power Down Current from Digital	IVDD	Power down	NA	1	NA	uA

3.10 Electrical Characteristics for MIPI DPHY TX

Table 3-10 Electrical Characteristics for MIPI DPHY TX

Parameters	Symbol	Test condition	Min	Typ	Max	Units
HS TX static common-mode	Vcmtx		150	200	250	mV
Vcmtx mismatch when output is Differential-1 or Differential-0	ΔVcmtx(1,0)		NA	NA	5	mV
HS Transmit differential voltage	Vod		140	200	270	mV
Vod mismatch when output is Differential-1 or Differential-0	ΔVod		NA	NA	14	mV
HS output high voltage	Vohhs		NA	NA	360	mV
Single ended output impedance	Zos		40	50	62.5	Ohm
Single ended output impedance mismacth	ΔZos		NA	NA	10	%
The venin output high level	Voh		1.08	1.2	1.32	V
The venin output low level	Vol		-50	NA	50	mV
Output impedance of LP	Zolp		110	NA	NA	Ω
High-level output voltage	Voh		1.62	1.8	NA	V
Low-level output voltage	Vol		NA	0	0.2	V
Output impedance	Zolp		40	NA	460	Ω
Common-mode variations above 450 MHz	ΔVcmtx(HF)		NA	NA	15	mVrms
Common-mode variations between 50MHz – 450MHz	ΔVcmtx(LF)		NA	NA	25	mVpeak
20%-80% rise time and fall time	Tr and Tf		NA	NA	0.3	UI
			100	NA	NA	ps
Maximum data rate	Dmax		NA	200	NA	Mbit/s
15%-85% rise time and fall time	Trlp/Tflp		NA	NA	2.5	ns
Slew rate, transition region	SR		150	250	500	mV/ns

3.11 Electrical Characteristics for MIPI DPHY RX

Table 3-11 Electrical Characteristics for MIPI DPHY RX

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Common-mode voltage HS receive mode	Vcmrx(dc)		70		300	mV
Differential input high threshold	Vidth				70	mV
Differential input low threshold	Vidtl		-70	NA	NA	mV
Single-ended input high voltage	Vihhs		NA	NA	460	mV
Single-ended input low voltage	Vilhs		-40	NA	NA	mV

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Single-ended threshold for HS termination enable	Vterm-en		NA	NA	450	mV
Differential input impedance	Zid		80	100	125	Ω
Logic 1 input voltage	Vih	<=1.5Gbps	880	NA	NA	mV
		>1.5Gbps	740	NA	NA	mV
Logic 0 input voltage, not in ULP state	Vil		NA	NA	550	mV
Logic 0 input voltage, ULP state	Vil-ulps		NA	NA	300	mV
Input hysteresis	Vhyst		25	NA	NA	mV
Common-mode interference beyond 450 MHz	ΔVcmrx(HF)		NA	NA	100	mV
Common-mode interference 50MHz-450MHz	ΔVcmrx(LF)		-50	NA	50	mV
Common-mode termination	Ccm		NA	NA	60	pF
Input pulse rejection	Espike		NA	NA	300	V.ps
Minimum pulse width response	Tmin-rx		20	NA	NA	ns
Peak interference amplitude	Vint		NA	NA	200	mV
Interference frequency	Fint		450	NA	NA	MHz

3.12 Electrical Characteristics for PCIe

Table 3-12 Electrical Characteristics for PCIe Transmitter

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Unit interval	UI		199.94	200	200.06	Ps
Differential Peak to Peak	VTX-DIFFp-p		800	NA	1200	mV pk-pk
Low-Drive Differential Peak to Peak Output Voltage	VTX-DIFFp-pLOW		400	NA	1200	mV pk-pk
De-Emphasized Differential Output Voltage Ratio	VTX-DE-RATIO-3.5dB		-3.0	-3.5	-4.0	dB
Minimum Instantaneous Lone Pulse Width	TMIN-PULSE		0.9	NA	NA	UIpk-pk
Minimum TX Eye Width: TJ=14*RJ+DJ	TTX-EYE		0.75	NA	NA	UI
Transmitter Deterministic Jitter > 1.5MHz Bandwidth	TTX-HF-DJ-DD		NA	NA	0.15	UIpk-pk
Rise/Fall Time Differential Mismatch	TRF-MISMATCH		NA	NA	0.1	UI
Peak-Peak AC Common Mode Voltage Variation	VTX-CM-ACpp		NA	NA	100	mVpk-pk
PLL Transfer Function Peaking	Peaking-PLL		NA	NA	1/3	dB
Differential Return Loss	RLTX-DIFF		10dB:0.05 –1.25GHz; 8dB: 1.25 –2.5GHz	NA	NA	dB
Common Mode Return Loss	RLTX-CM		NA	NA	6	dB
DC Differential TX DC	ZTX-DIFF-DC		NA	NA	120	Ω

Table 3-13 Electrical Characteristics for PCIe Receiver

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Differential Input Eye Height			100	NA	2000	mVdiffpp
Differential DC return loss			20	NA	NA	dB
Differential AC return loss			~10	NA	NA	dB
Command mode DC return loss			18	NA	NA	dB
Command mode AC return loss			6	NA	NA	dB
DC input differential termination			80	NA	110	Ω
Power down DC input impedance			200	NA	NA	kΩ
Input common mode AC voltage peak-peak			NA	NA	200	mVp
Jitter Tolerance(TJ)			0.8	NA	NA	UIpp
Jitter Tolerance(RJ)			1.5	NA	NA	ps RMS
Jitter Tolerance(DJ)			0.65	NA	NA	UIpp

Table 3-14 External Reference Clock Specification for PCIe

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Rising edge rate	TC-RISE	Differential	0.6	NA	4	V/ns
Falling edge rate	TC-FALL	Differential	0.6	NA	4	V/ns
Differential input high voltage	VIH	Differential	150	NA	NA	mV
Differential input low voltage	VIL	Differential	NA	NA	-150	mV
Absolute single ended crossing point voltage	VCROSS	Single-ended	250	NA	550	mV
Variation of VCROSS over all rising clock edges	VCROSS-DELTA	Single-ended	NA	NA	+140	mV
Ring back voltage margin	VRB	Differential	-100	NA	+100	mV
Time before VRB is allowed	TSTABLE	Differential	500	NA	NA	ps
Average clock period accuracy	TPERIOD-AVG		-300	NA	2800	ppm
Absolute period, including spread-spectrum and jitter	TPERIOD-ABS		9.847	NA	10.203	ns
Cycle to cycle jitter	TCC-JITTER		NA	NA	150	ps
Absolute maximum input voltage	VMAX		NA	NA	1.15	v
Absolute MINIMUM input voltage	VMIN		-0.3	NA	NA	v
Duty cycle			45	NA	55	%
Single ended rising refclk edge rate versus falling refclk edge rate	Rise/Fall Matching		NA	NA	20	%
Clock source output DC impedance	ZC-DC		40	NA	60	Ω

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Rising edge rate(10%-90%)	TC-RISE		NA	NA	0.05	RCUI
Falling edge rate(90%-10%)	TC-FALL		NA	NA	0.05	RCUI
Rise/Fall mismatch			NA	NA	20	%
Input voltage level-CMOS	VSE		0	NA	0.9	V
Average clock period accuracy	TPERIOD-AVG		-300	NA	+300(2800 Including SSC)	ppm
Reference Clock Frequency	FREF		NA	100	NA	MHZ

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Typical	Unit
Junction-to-ambient thermal resistance	$\boldsymbol{\theta_{JA}}$	27.3	(℃/$\boldsymbol{W}$)
Junction-to-board thermal resistance	$\boldsymbol{\theta_{JB}}$	NA	(℃/$\boldsymbol{W}$)
Junction-to-case thermal resistance	$\boldsymbol{\theta_{JC}}$	NA	(℃/$\boldsymbol{W}$)

Note: The testing PCB is 6 layers, 75mmx153mm, 1.6mm thickness, Ambient temperature is 25℃.